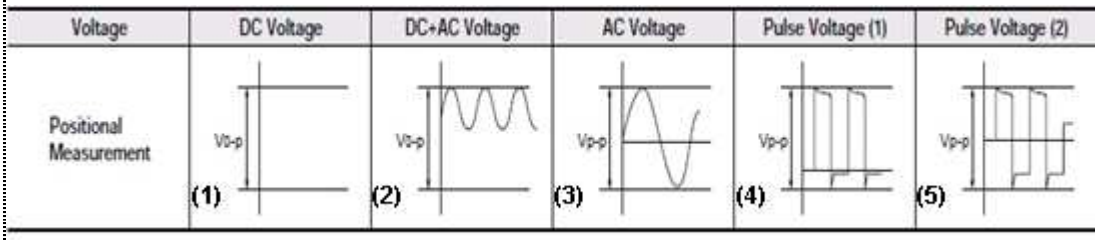
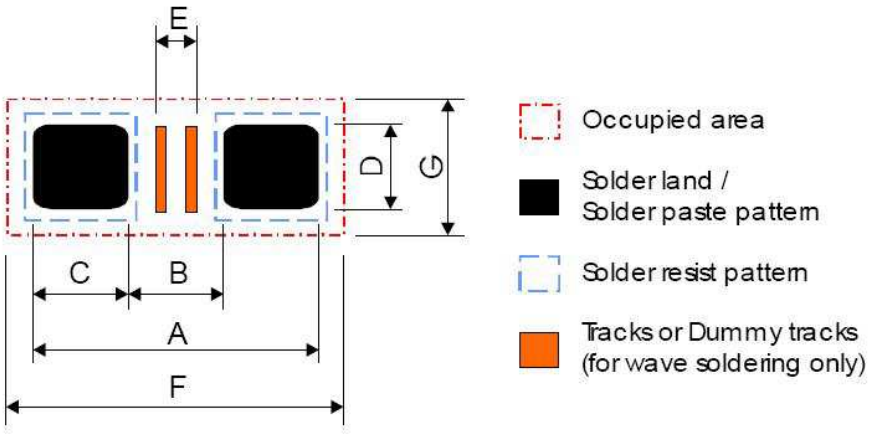
MLCC
APPLICATION GUIDE

No.	Process	Condition
1	**Operating Condition (Storage)**	1) The capacitor must be stored in an ambient temperature between 5 ~ 40℃ with a relative humidity of 20 ~ 70%. The products should be used within 12 months upon receipt. 2) The capacitors must be operated and stored in an environment free of dew condensation and these gases such as Hydrogen Sulphide, Hydrogen Sulfate, Chlorine and Ammonia and sulfur. 3) Avoid storing in direct sunlight and falling of dew. 4) Do not use capacitors under high humidity and high and low atmospheric pressure which may affect capacitors reliability.
2	**Circuit design** **! Caution**	2-1 Operating temperature Operating temperature should be followed strictly within this specification, especially be careful with maximum temperature. 1) Do not use capacitor above the maximum allowable operating temperature. 2) Surface temperature including self heating should be below maximum operating temperature. (Due to dielectric loss, capacitor will heat itself when AC is applied. Especially at high frequencies around its SRF, the heat might be so extreme that it may damage itself or the surrounding area. Please design the circuit so that the maximum temperature of the capacitor including the self heating to be below the maximum allowable operating temperature. Temperature rise shall be below 20℃) 2-2 Operating voltage 1) Operating voltage across the terminals should be below the rated voltage. When AC and DC are super imposed, the peak must be below the rated voltage. With AC or pulse overshooting, Vp-p must be below the rated voltage. ----------(1)&(2) AC or Pulse with overshooting, Vp-p must be below the rated voltage. ----------(3),(4)&(5) When the voltage is started to apply to the circuit or it is stopped applying, the irregular voltage may be generated for a transit period because of resonance or switching. Be sure to use a capacitor within rated voltage containing these irregular voltage.  2) Even below the rated voltage, if repetitive high frequency AC or pulse is applied, the reliability of the capacitor may be reduced. 3) Voltage derating will greatly reduce the failure rate. Since the failure rate follows the 3 power law of voltage, the failure rate used under Uw with UR rated product will be lowered as $(Uw/UR)^3$.

No.	Process	Condition
3	Designing P.C. board	The amount of solder at the terminations has a direct effect on the reliability of the capacitor. 1) The greater the amount of solder, the higher the stress on the chip capacitor, and the more likely that it will break. When designing a P.C. board, determine the shape and size of the solder pads to have proper amount of solder on the terminations. 2) Avoid using common solder pads for multiple terminations and provide individual solder pads for each terminations. See the following table for recommended pad dimensions.



Reflow Soldering

SIZE	Footprint dimensions in mm							Processing remarks	Placement Accuracy
	A	B	C	D	E	F	G		
01005	0.45	0.20	0.15	0.21	N/A	0.65	0.38	Reflow or hot plate soldering	± 0.05
0201	0.65	0.23	0.21	0.30	N/A	0.90	0.60		± 0.05
0402	1.50	0.40	0.50	0.50	0.10	1.75	0.95		± 0.15
0508	2.50	0.50	1.00	2.00	0.15	2.90	2.40		± 0.20
0505	3.43	0.94	1.42	2.11	N/A	N/A	N/A		± 0.25
0603	2.30	0.70	0.80	0.80	0.20	2.55	1.40		± 0.25
0612	2.80	0.80	1.00	3.20	0.20	3.08	3.85		± 0.25
0805	2.80	1.00	0.90	1.30	0.40	3.05	1.85		± 0.25
1111	4.62	2.01	1.42	3.45	N/A	N/A	N/A		± 0.25
1206	4.00	2.20	0.90	1.60	1.60	4.25	2.25		± 0.25
1210	4.00	2.20	0.90	2.50	1.60	4.25	3.15		± 0.25
1808	5.40	3.30	1.05	2.30	2.70	5.80	2.90		± 0.25
1825	5.30	3.50	0.90	6.50	N/A	N/A	N/A		± 0.30
1812	5.30	3.50	0.90	3.80	3.00	5.55	4.05		± 0.25
2211	7.00	4.30	1.35	3.70	N/A	7.60	4.10		± 0.30
2220	7.00	4.30	1.35	5.00	N/A	7.60	5.50		± 0.30
2225	7.00	4.30	1.35	6.50	N/A	N/A	N/A		± 0.40

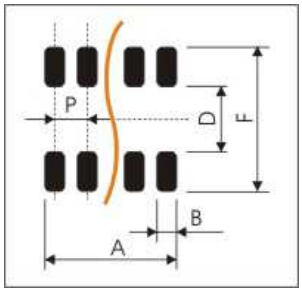
No.	Process	Condition
3	Designing P.C. board (Continued)	

Wave Soldering

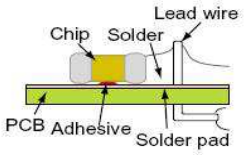
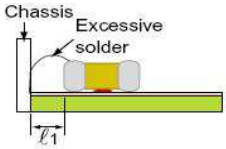
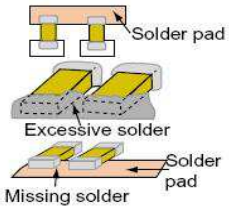
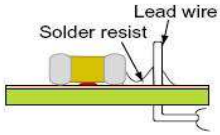
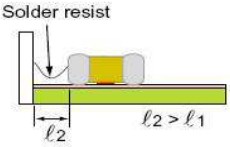
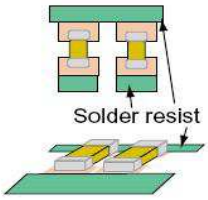
SIZE	Footprint dimensions in mm							Proposed number & Dimensions of dummy tracks	Placement Accuracy
	A	B	C	D	E	F	G		
0603	2.40	1.00	0.70	0.80	0.20	3.10	1.90	1x (0.20x0.80)	± 0.10
0805	3.20	1.40	0.90	1.30	0.36	4.10	2.50	1x (0.30x1.30)	± 0.15
1206	4.80	2.30	1.25	1.70	1.25	5.90	3.20	3x (0.25x1.70)	± 0.25
1210	5.30	2.30	1.50	2.60	1.25	6.30	4.20	3x (0.25x2.60)	± 0.25

Footprint design for C Array :

Type	0603*4	0402*4
A	2.85 +0.10/-0.05	1.80 ± 0.10
B	0.45 ± 0.05	0.25 ± 0.05
D	0.80 ± 0.10	0.65 ± 0.05
P	0.80	0.50
F	3.10 ± 0.30	1.85 ± 0.25

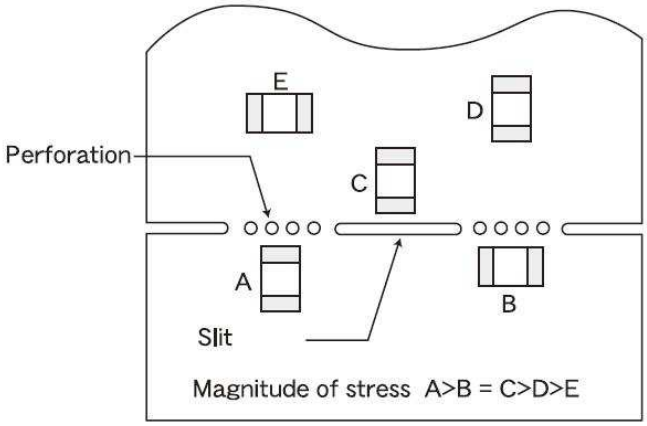


3) Layout recommendation

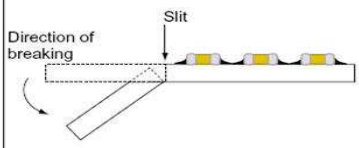
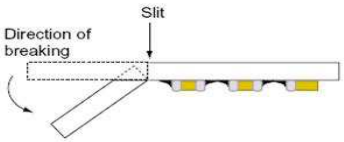
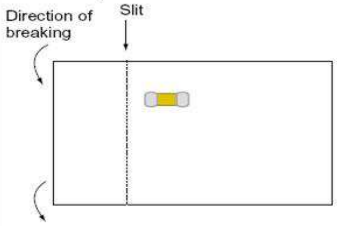
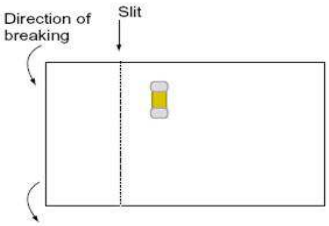
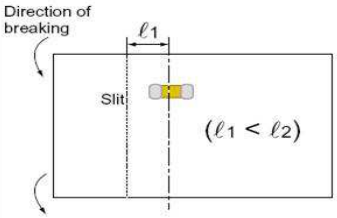
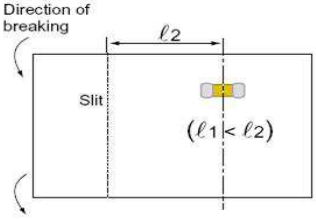
Example	Use of common solder land	Soldering with chassis	Use of common solder land with other SMD
Must be avoided			
Recommended			

3 Designing P.C. board (Continued)

4) Mechanical stress varies according to location of chip capacitors on the P.C. board.



5) Recommended chip capacitor layout is as follows:

Subject	Disadvantage against bending stress	Advantage against bending stress
Mounting face	Perforation & slit  Break P.C. board with mounted side up	Perforation & slit  Break P.C. board with mounted side down.
Chip arrangement (Direction)	Mount perpendicular to perforation or slit 	Mount in parallel with perforation or slit 
Distance from slit	Closer to slit is higher stress 	Away from slit is less stress 

4 Mounting

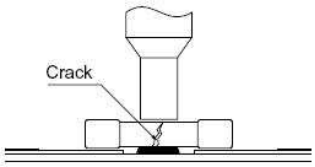
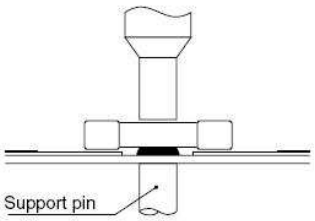
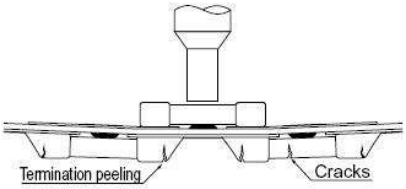
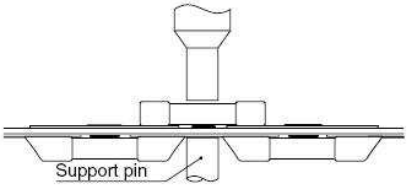
4-1 Stress from mounting head

If the mounting head is adjusted too low, it may induce excessive stress in the chip Capacitor resulting in cracking. Please take the following precautions.

1) Adjust the bottom dead center of the mounting head to just on the P.C. board surface and not pressing on it.

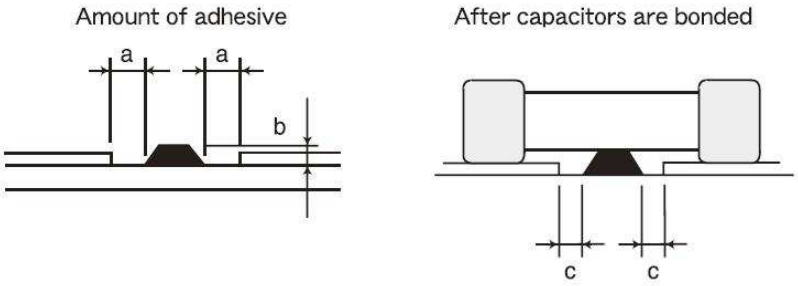
2) Adjust the mounting head pressure to be 1 to 3N of static weight.

3) To minimize the impact energy from mounting head, it is important to provide support from the bottom side of the P.C. board.(see following)

Mounting	Not recommended	Recommended
Single sided		
Double sided		

When the centering jaw is worn out, it may give mechanical impact on the capacitor to cause a crack. Please control the close up dimension of the centering jaw and provide sufficient preventive maintenance and replacement of it.

4-2 Amount of adhesive



Example : 0805(2012) and 1206(3216)

Figure	0805/1206 case sizes as examples
a	0.2mm min
b	70 ~ 100 um
c	Do not touch the solder land

5 Soldering

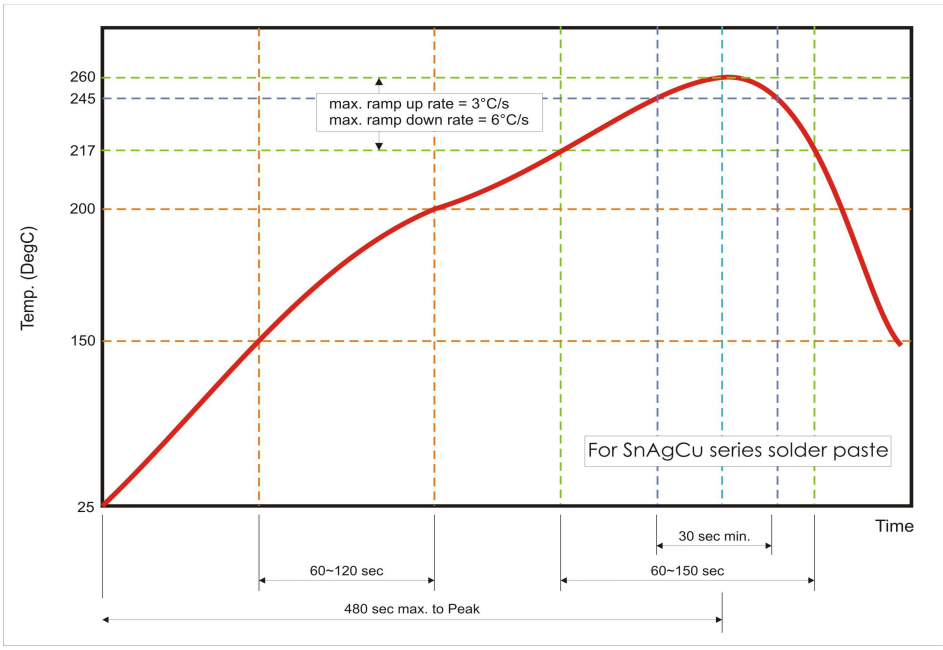
5-1 Flux selection

Although highly-activated flux gives better solderability, substances which increase activity may also degrade the insulation of the chip capacitors. To avoid such degradation, the following is recommended.

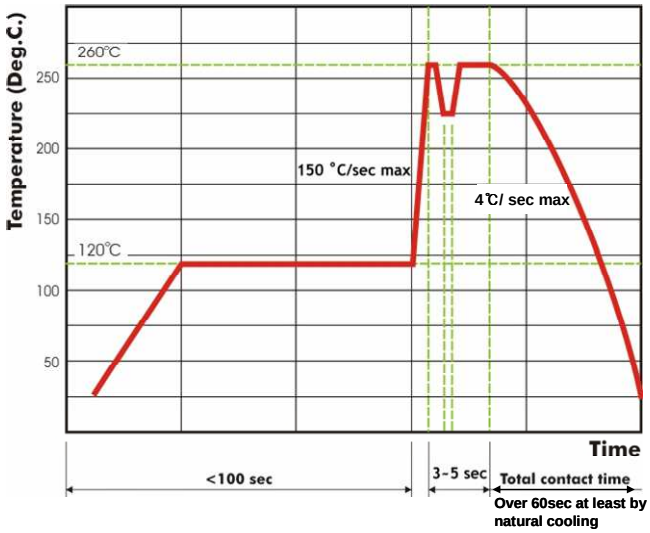
1) It is recommended to use a mildly activated rosin flux (less than 0.1 wt% chlorine). Strong flux is not recommended.
2) Excessive flux must be avoided. Please provide proper amount of flux.
3) When water-soluble flux is used, enough washing is necessary.

5-2 Recommended soldering profile by various methods

1) Recommended reflow soldering profile for SMT process with SnAgCu series solder paste



2) Wave soldering profile

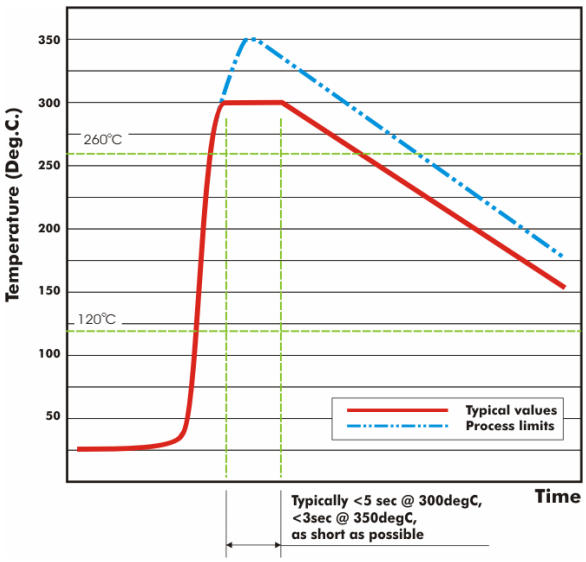


Recommended wave soldering profile for SMT process with SnAgCu series solder.

Wave soldering is recommended only for the following case sizes:
0603(1608); 0805(2012) &1206(3216) thickness< 1mm

5 Soldering (Continued)

3) Manual soldering (solder iron)



5-3 Avoiding thermal shock

1) Preheating condition

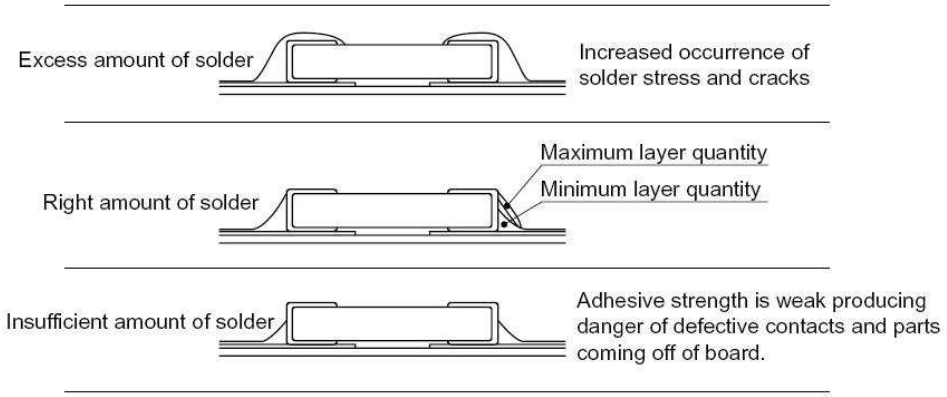
Soldering	Size	Temperature difference(ΔT)
Wave soldering	1206 (3216) or less	ΔT ≦ 150℃
Reflow soldering	1206 (3216) or less	ΔT ≦ 190℃
	1210 (3225) or more	ΔT ≦ 130℃
Manual soldering	1206 (3216) or less	ΔT ≦ 190℃
	1210 (3225) or more	ΔT ≦ 130℃

2) Cooling condition

Natural cooling using air is recommended. If the chips are dipped into a solvent for cleaning, the temperature difference (ΔT) must be less than 100℃.

5-4 Amount of solder

Excessive solder will induce higher tensile force in chip capacitor when temperature changes and may result in chip cracking. Insufficient solder may detach the capacitor from the P.C. board.



5-5 Two times limitation for reflow soldering will be recommended.

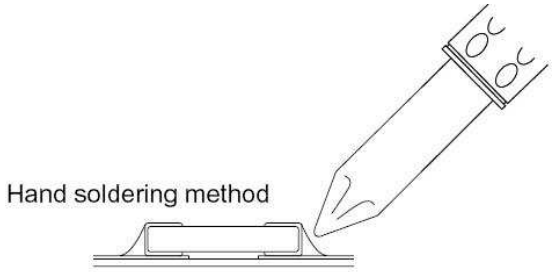
5-6 Solder repair by solder iron

1) Selection of the soldering iron tip

Tip temperature of solder iron varies by its type, P.C. board material and solder pad size. Higher tip temperature may be faster, but the heat shock may crack the chip capacitor. (Following conditions are recommended.)

Size	Temp. (℃)	Preheating Temp. (℃)	Temperature difference(ΔT)	Atmosphere
1206 (3216) or less	350℃ Max	>150℃	ΔT ≦ 190℃	Room air
1210 (3225) or more	280℃ Max	>150℃	ΔT ≦ 130℃	Room air

2) Direct contact of the soldering iron with ceramic dielectric of chip capacitor may cause cracking. Do not make contact directly with the ceramic dielectric.



6 Cleaning

1) If an unsuitable cleaning fluid is used, flux residue or some foreign article may stick to chip capacitor surface causing deteriorated performance, especially insulation resistance.

2) If the cleaning condition is not suitable, it may damage the chip capacitor.

2-1) Insufficient washing

(1) Lead wire and terminal electrodes may corrode due to Halogen in the flux.
(2) Halogen in the flux may adhere on the surface of capacitor, and lower the insulation resistance.
(3) Water soluble flux has higher tendency to have the above mentioned problems (1) and (2).

2-2) Excessive washing

When ultrasonic cleaning is used, excessively high ultrasonic energy output can affect the connection between the ceramic chip capacitor's body and the terminal electrode. To avoid this, use the following recommended condition.

Power : 20W/l max.
Frequency : 40kHz max.
Washing time : 5 minutes max.

2-3) If the cleaning fluid is contaminated, the density of Halogen increases, and it may bring the same result as insufficient cleaning.

3) Selection of cleaning fluid

In general, washing is not necessary if rosin-based flux is used. When using active flux, suitable cleaning fluids are water, isopropyl or a solvent that has the capability to remove the flux.

4) Precautions

After the reflow process, wait at least 5 minutes before proceeding with the cleaning procedure.

7 Coating and molding of the P.C. board

1) When the P.C. board is coated, verify the quality influence on the product.

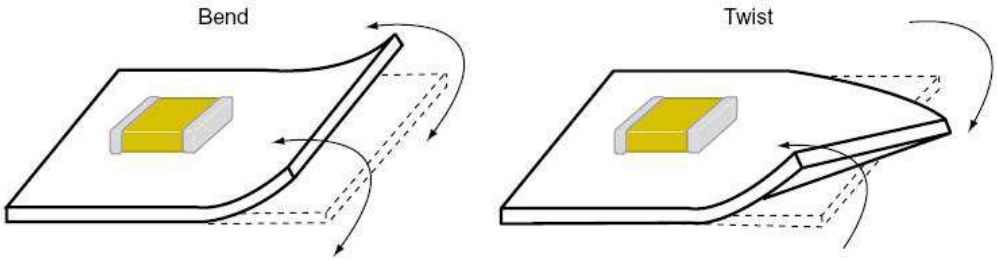
2) Please verify that there is no harmful decomposing or reaction gas emission during curing which may damage the chip capacitor.

3) Please verify the curing temperature.

8 Handling after chip is mounted

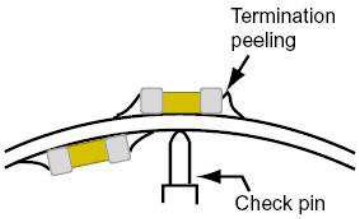
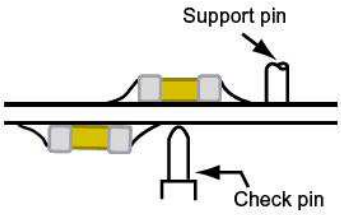
1) Please pay attention not to bend or distort the P.C. board after soldering in handling and storage, otherwise the chip capacitor may crack .

Avoid the following:



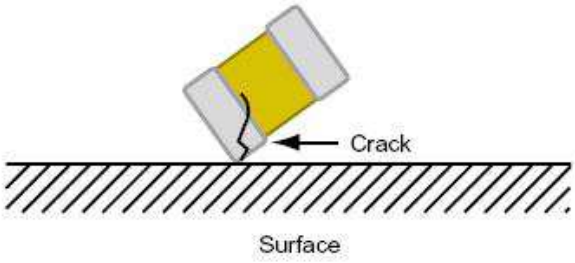
2) When functional check of the P.C. board is performed, check pin pressure as it tends to be adjusted higher for fear of loose contact. If the pressure is excessive and bends the P.C. board, it may crack the chip capacitor or peel the terminations off.

Adjust the check pins not to bend the P.C. board.

Item	Not recommended	Recommended
Board bending		

9 Handling of loose chip capacitor

1) If dropped the chip capacitor may crack. Once dropped do not use it. This is especially true for large case sized chips.



2) Avoid piling up P.C. boards after mounting. The corner of the P.C. board may hit the chip capacitor of another board causing the chip to crack or dislodge.