



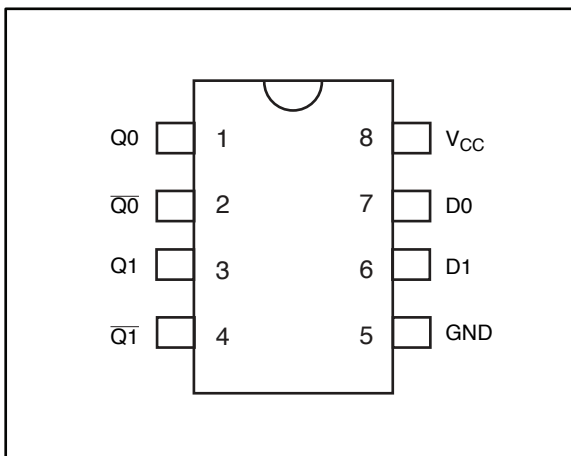
PO100HSTL22A

Dual LVTTTL/LVCMOS to Differential HSTL Translator

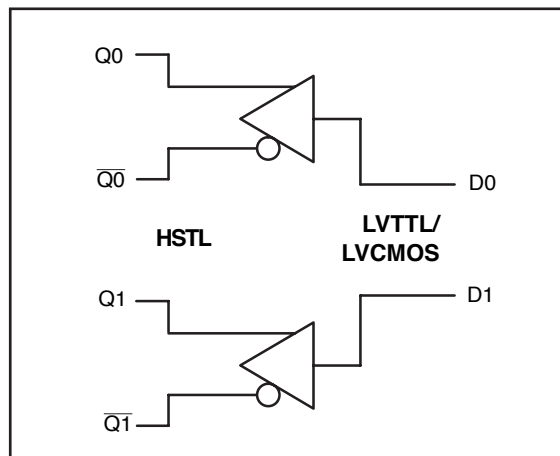
High Frequency Noise Cancellation Translator

FEATURES:	DESCRIPTION:
• Patented Technology • HSTL differential outputs • LVTTTL/LVCMOS to Differential HSTL Translator • Operating frequency up to 1.65GHz with 5pf load • Operating frequency up to 500MHz with 15pf load • Very low output pin to pin skew < 100ps • Propagation delay < 1.4ns max with 15pf load • 1.65V to 3.6V power supply • Industrial temperature range: -40°C to 85°C • Available in 8-pin SOIC package • Available in 8-pin TSSOP package	Potato Semiconductor's PO100HSTL22A is designed for world top performance using submicron CMOS technology to achieve 1.65GHz HSTL output frequency with less than 1.4ns propagation delay. The PO100HSTL22A is a low-skew, LVTTTL/LVCMOS to Differential HSTL Translator. The small outline 8 pin package and the low skew design to make it ideal for applications which require the translation of a clock or a data signal.

Pin Configuration



Logic Block Diagram



Pin Description

PIN	FUNCTION
Qn, Qn̄	HSTL Differential Outputs
D0, D1	LVTTTL/LVCMOS Inputs
V _{CC}	Positive Supply
GND	Ground

**High Frequency Noise Cancellation Translator****Maximum Ratings**

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:

stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
VOH	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
VOL	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
VIH	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	Vcc	V
VIL	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
IIH	Input High current	Vcc = 3.6V and Vin = 5.5V	-	-	1	uA
IIL	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
VIK	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

**High Frequency Noise Cancellation Translator****Power Supply Characteristics**

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
IccQ	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

Notes:

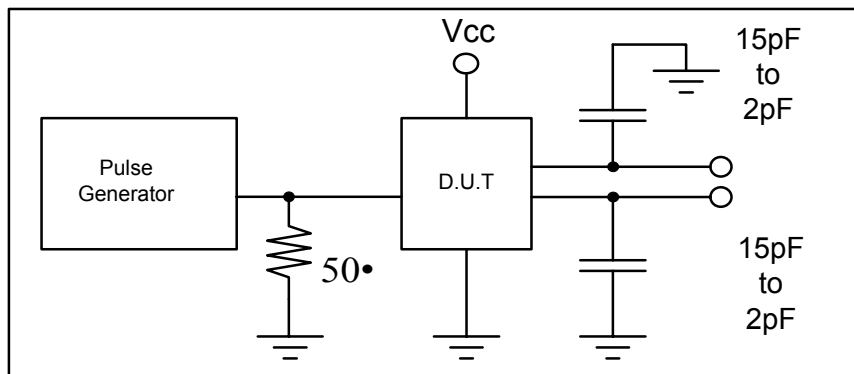
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Typ	Max	Unit
tpD	Propagation Delay D to Output pair	CL = 15pF		1.4	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V		0.8	ns
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz		100	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz		250	ps
tJITTER	Random Clock Jitter (RMS)	CL = 15pF, 125MHz	1.6		ps
fmax	Input Frequency	CL = 15pF		500	MHz
fmax	Input Frequency	CL = 5pF		1.65	GHz

Notes:

1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Circuit



High Frequency Noise Cancellation Translator

Test Waveforms

FIGURE 1.
LVTTTL/LVCMOS INPUT WAVEFORM DEFINITION

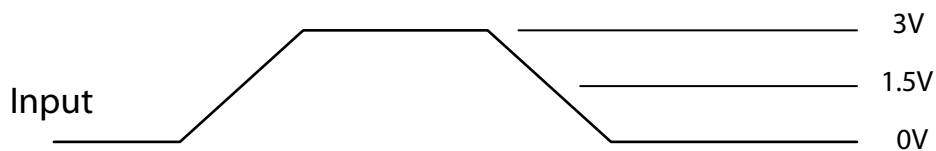


FIGURE 2.
HSTL OUTPUT

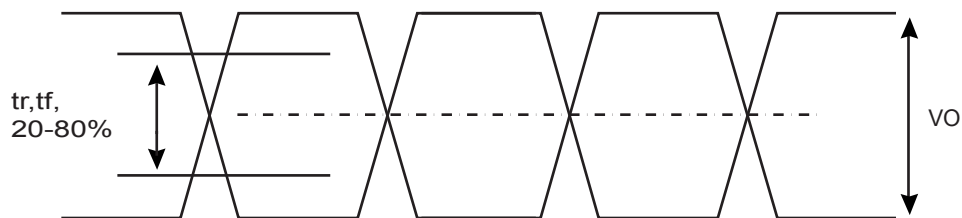
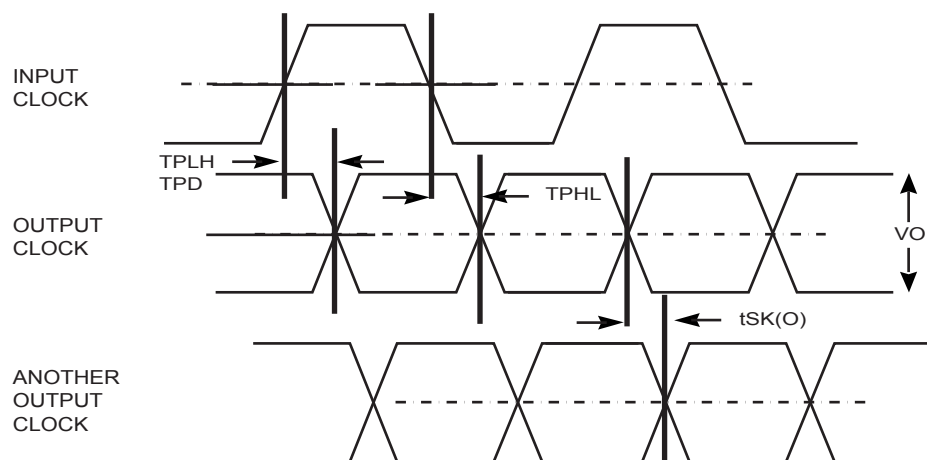
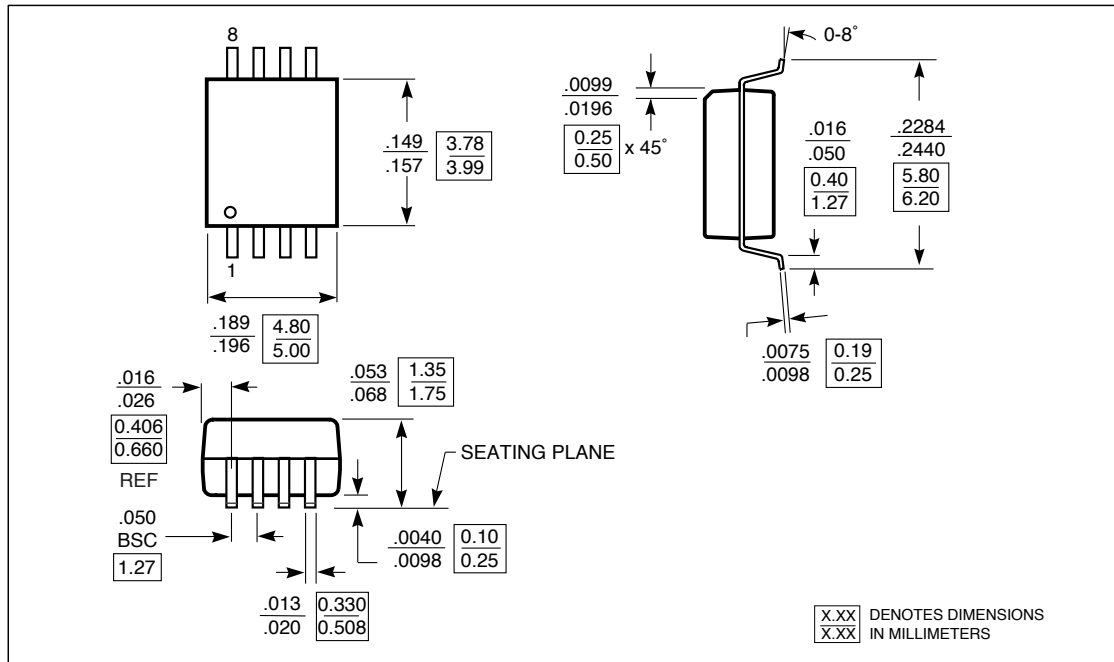


FIGURE 3.
Propagation Delay, Output pulse skew, and output-to-output skew for D to output pair

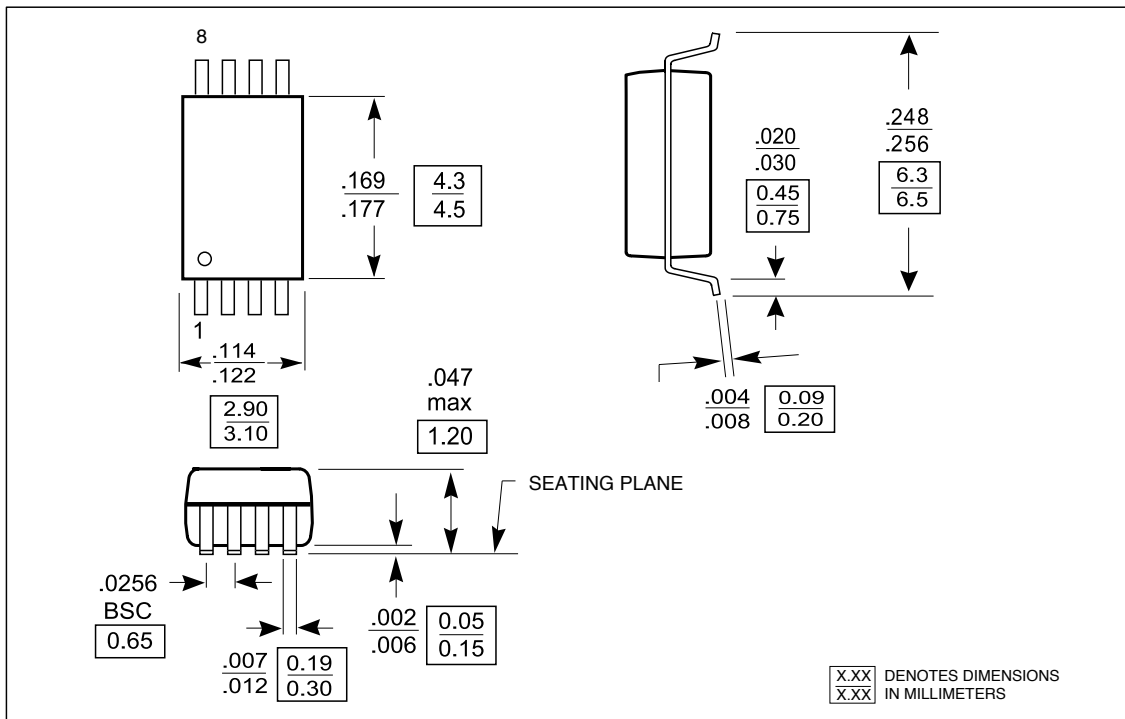


High Frequency Noise Cancellation Translator

Packaging Mechanical Drawing: 8 pin SOIC



Packaging Mechanical Drawing: 8 pin TSSOP





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IC Ordering Information

Ordering Code	Package		Top-Marking	T _A
PO100HSTL22ASU for Tube	8 pin 150mil SOIC	Pb-free & Green	PO100HSTL22AS	-40°C to 85°C
PO100HSTL22ASR for Tape & Reel	8 pin 150mil SOIC	Pb-free & Green	PO100HSTL22AS	-40°C to 85°C
PO100HSTL22ATU for Tube	8 pin 173mil TSSOP	Pb-free & Green	PO100HSTL22TS	-40°C to 85°C
PO100HSTL22ATR for Tape & Reel	8 pin 173mil TSSOP	Pb-free & Green	PO100HSTL22TS	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	TAPE & REEL PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER TAPE	TAPE LEADER LENGTH	QTY PER TUBE
S	8-pin 150mil SOIC	12	8	Top Left Corner	39 (12")	3000	64 (20")	97
T	8-pin 173mil TSSOP	12	8	Top Left Corner	39 (12")	3000	64 (20")	158