

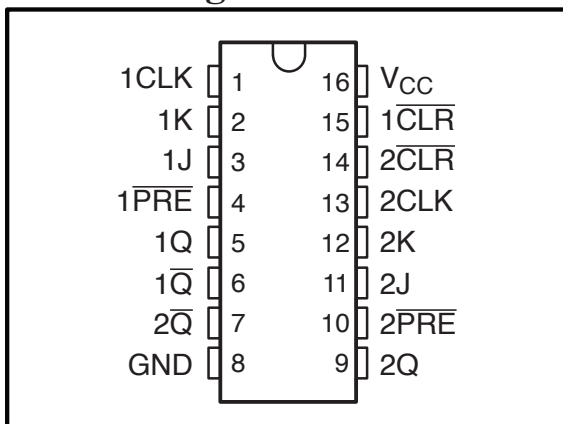
**74 Series Noise Cancellation GHz Logic****FEATURES:**

- Patented technology
- Specified From -40°C to 85°C , -40°C to 125°C , and -55°C to 125°C
- Operating frequency up to 750MHz with 15pf load
- VCC Operates from 1.65V to 3.6V
- Propagation delay < 2ns max with 15pf load
- Low input capacitance: 4pf typical
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
- 5000-VHuman-BodyModel (A114-A)
- 200-VMachineModel (A115-A)
- Available in 16pin 150mil wide SOIC package
- Available in 16pin 173mil wide TSSOP package

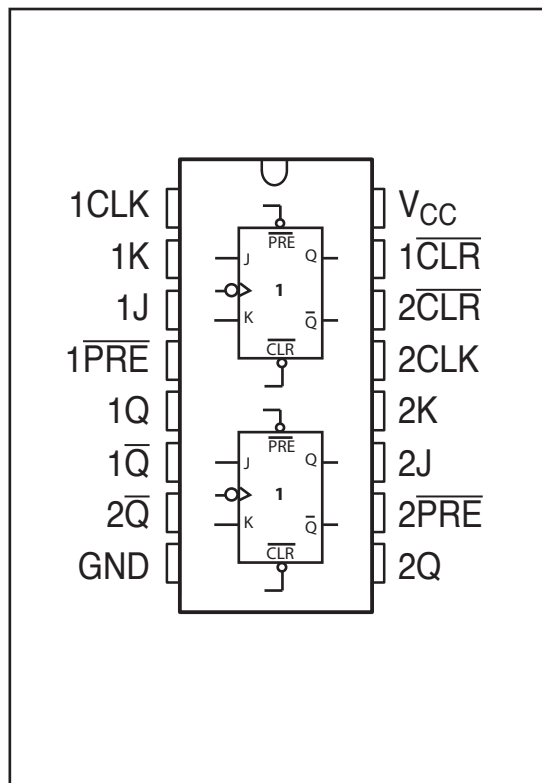
DESCRIPTION:

Potato Semiconductor's PO74G112A is designed for world top performance using submicron CMOS technology to achieve 750MHz TTL /CMOS output frequency with less than 2ns propagation delay. This dual negative-edge-triggered J-K flip-flop is designed for 1.65-V to 3.6-V Vcc operation.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

Pin Configuration**Pin Description**

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q ₀	Q̄ ₀

Logic Block Diagram

**74 Series Noise Cancellation GHz Logic****Maximum Ratings**

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-55 to 125	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to V _{cc} +0.5	V

Note:

stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	V _{cc} =3V Vin=V _{IH} or V _{IL} , I _{OH} = -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	V _{cc} =3V Vin=V _{IH} or V _{IL} , I _{OH} =12mA	-	0.3	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	5.5	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{IH}	Input High current	V _{cc} = 3.6V and Vin = 5.5V	-	-	1	uA
I_{IL}	Input Low current	V _{cc} = 3.6V and Vin = 0V	-	-	-1	uA
V_{IK}	Clamp diode voltage	V _{cc} = Min. And I _{IN} = -18mA	-	-0.7	-1.2	V

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{cc} = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. V_{OH} = V_{cc} – 0.6V at rated current

**74 Series Noise Cancellation GHz Logic****Power Supply Characteristics**

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
IccQ	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	40	uA

Notes:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Capacitance

Parameters (1)	Description	Test Conditions	Typ	Unit
Cin	Input Capacitance	Vin = 0V	4	pF
Cout	Output Capacitance	Vout = 0V	6	pF

Notes:

- 1 This parameter is determined by device characterization but not production tested.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Min	Unit
tsu	Setup time before CLK ↑		-	0.5	ns
th	Hold time, data after CLK ↑		-	0.5	ns
tPLH	Propagation Delay CLK to Q or $\overline{Q}$	CL = 15pF	2	-	ns
tPHL	Propagation Delay CLK to Q or $\overline{Q}$	CL = 15pF	2	-	ns
tPLH	Propagation Delay $\overline{CLR}$ or $\overline{PRE}$ to Q or $\overline{Q}$	CL = 15pF	3	-	ns
tPHL	Propagation Delay $\overline{CLR}$ or $\overline{PRE}$ to Q or $\overline{Q}$	CL = 15pF	3	-	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	-	ns
fmax	Input Frequency	CL=2pF - 15pF	750	-	MHz

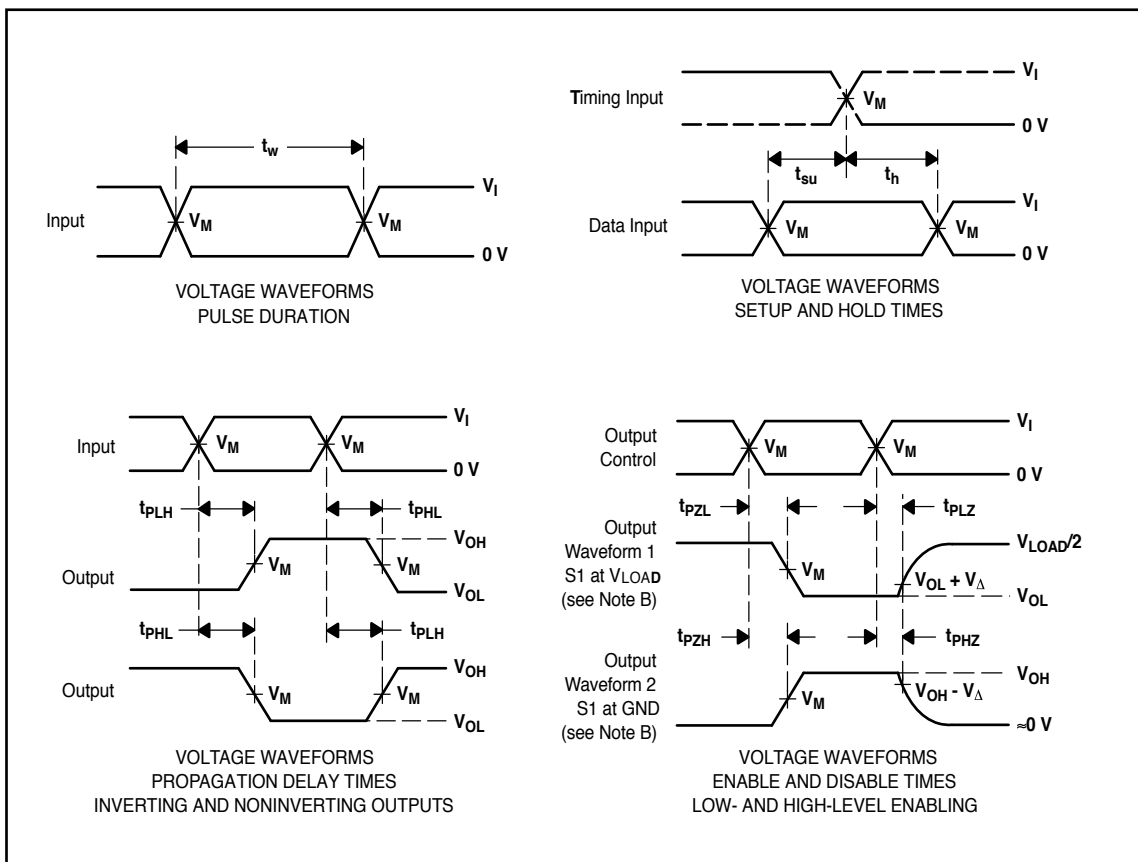
Notes:

1. See test circuits and waveforms.
2. tPLH, tPHL, tsu, and th are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 500MHz

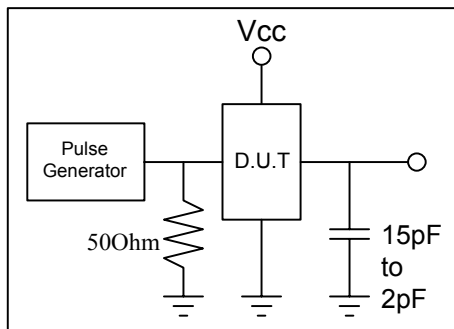


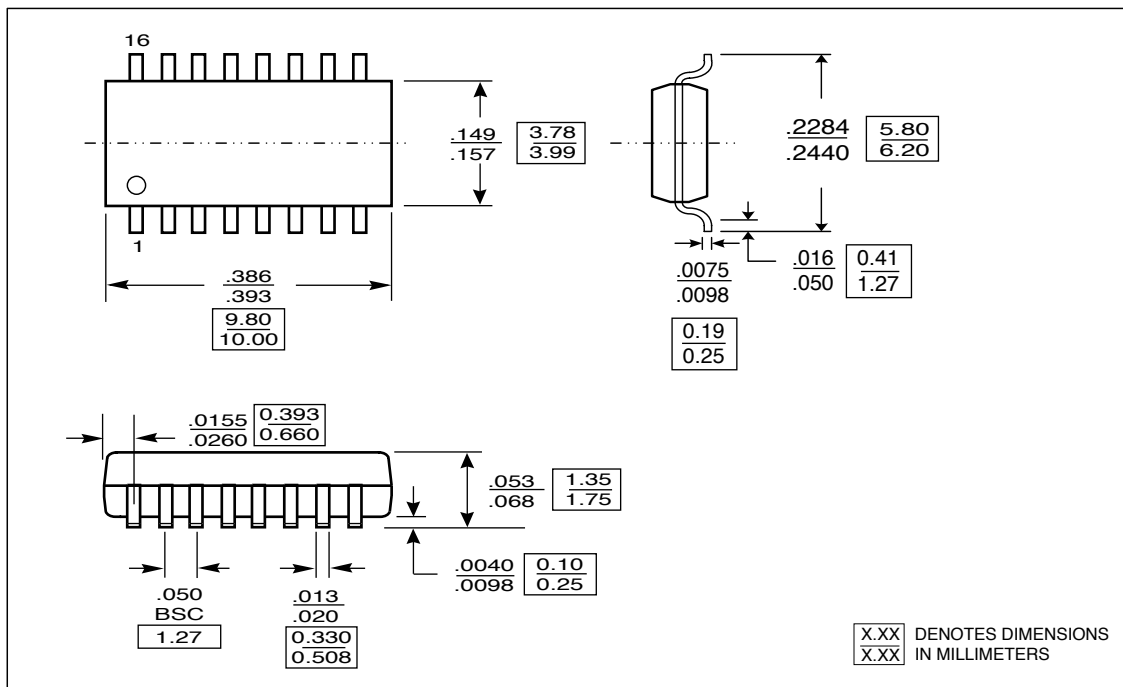
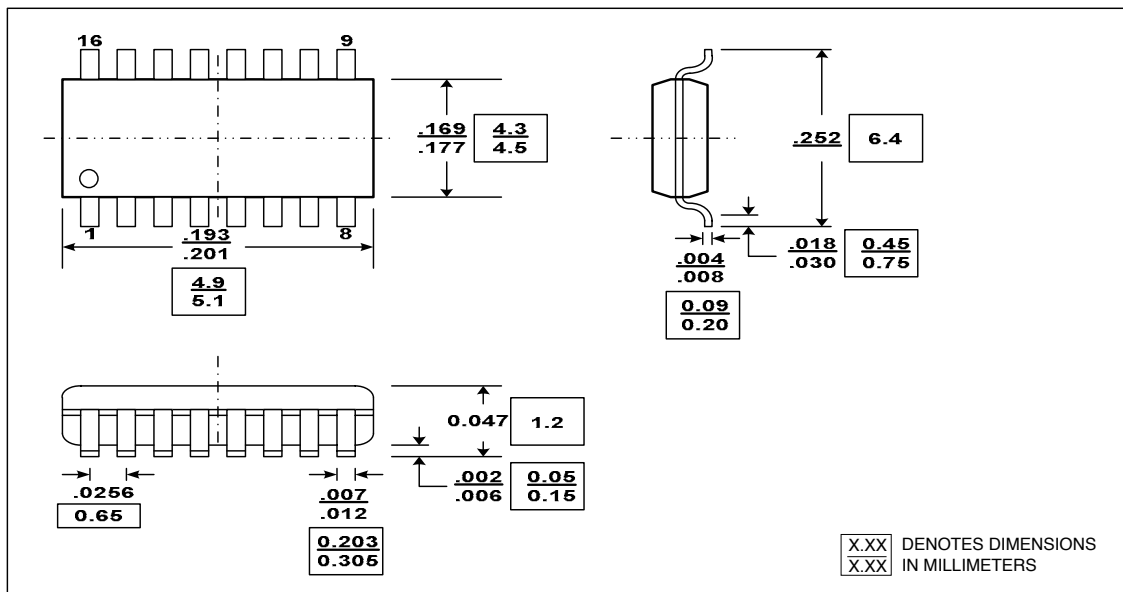
74 Series Noise Cancellation GHz Logic

Test Waveforms



Test Circuit



**74 Series Noise Cancellation GHz Logic****Packaging Mechanical Drawing: 16 pin SOIC****Packaging Mechanical Drawing: 16 pin TSSOP**



PO74G112A

DUAL NEGATIVE-EDGE-TRIGGERED J-K FLIP FLOP WITH CLEAR AND PRESET

74 Series Noise Cancellation GHz Logic

Ordering Information

Ordering Code	Package		Top-Marking	T _A
PO74G112ASU for Tube	150mil SOIC 16	Pb-free & Green	POTATO74G112AS	-40°C to 85°C
PO74G112ASR for Tape & Reel	150mil SOIC 16	Pb-free & Green	POTATO74G112AS	-40°C to 85°C
PO74G112ATU for Tube	173mil TSSOP 16	Pb-free & Green	POTATO74G112AT	-40°C to 85°C
PO74G112ATR for Tape & Reel	173mil TSSOP 16	Pb-free & Green	POTATO74G112AT	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER REEL	TAPE LEADER LENGTH	QTY PER TUBE
S	SOIC 16	16	8	Top Left Corner	39 (12")	3000	64 (20")	48
T	TSSOP 16	12	8	Top Left Corner	39 (12")	3000	64 (20")	96