PO74G553A

1.2V - 3.6V 1:4 CMOS Clock Buffered Driver

800MHz Noise Cancellation TTL/CMOS Potato Chip

FEATURES:

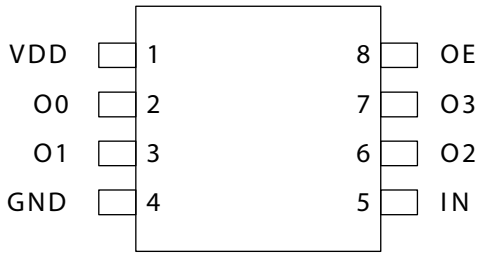
. Patented technology
. Operating frequency up to 800MHz with 2pf load
. Operating frequency up to 600MHz with 5pf load
. Operating frequency up to 300MHz with 15pf load
. Operating frequency up to 150MHz with 50pf load
. Very low output pin to pin skew < 50ps
. Very low pulse skew < 150ps
. VCC = 1.2V to 3.6V
. Propagation delay < 1.7ns max with 15pf load
. Low input capacitance: 3pf typical
. 1:4 fanout
. 5 V tolerant input clock
. Available in 8pin 150mil wide SOIC package

DESCRIPTION:

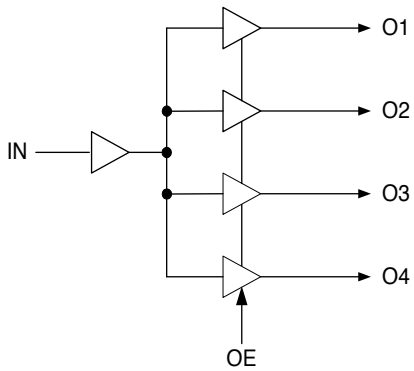
Potato Semiconductor's PO74G553A is designed for world top performance using submicron CMOS technology to achieve 800MHz TTL output frequency with less than 50ps output pulse skew.

PO74G553A is a CMOS 1 input to 4 outputs Buffered driver to achieve 800MHz Max output frequency. Typical applications are clock and signal distribution.

Pin Configuration



Logic Block Diagram



Pin Description

Pin Name	Description
IN	Signal or clock Inputs
OE	Hi-Z State Output Enable Inputs (Active LOW)
O1-O4	Signal or clock Outputs
GND	Ground
Vcc	Power

Inputs		Outputs
OE	IN	On
H	L	L
H	H	H
L	L	Z
L	H	Z

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Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to Vcc+0.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=VIH or VIL, IOH= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=VIH or VIL, IOH=12mA	-	0.3	0.5	V
V_{IH}	Input High voltage	Guaranteed Logic HIGH Level (Input Pin)	2	-	Vcc	V
V_{IL}	Input Low voltage	Guaranteed Logic LOW Level (Input Pin)	-0.5	-	0.8	V
I_{OZH}	High Impedance Output current	Vcc = 3.6V and Vo = Vcc	-	-	1	uA
I_{OZL}	High Impedance Output current	Vcc = 3.6V and Vo = 0V	-	-	-1	uA
I_{IH}	Input High current	Vcc = 3.6V and Vin = 3.6V	-	-	1	uA
I_{IL}	Input Low current	Vcc = 3.6V and Vin = 0V	-	-	-1	uA
V_{IK}	Clamp diode voltage	Vcc = Min. And IIN = -18mA	-	-0.7	-1.2	V

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

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Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25• C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Capacitance (T_A= +25°C, f= 1MHz)

Parameters (1)	Description	Test Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0V	3	4	pF
Cout	Output Capacitance	Vout = 0V	-	6	pF

Notes:
1 This parameter is determined by device characterization but not production tested.

Switching Characteristics

Symbol	Description	Test Conditions	Max	Unit
t_{PLH} & t_{PHL}	Propagation Delay INA to OAn, INB to OBn	CL = 15pF	1.7	ns
t_{PZH} or t_{PZL}	Output Enable Time	CL = 15pF	2.5	ns
t_{PHZ} or t_{PLZ}	Output Disable Time	CL = 15pF	2.5	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(p)	Pulse Skew (Same Package)	CL = 15pF, 125MHz	150	ps
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	0.25	ns
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	0.4	ns
fmax	Input Frequency	CL = 50pF	150	MHz
fmax	Input Frequency	CL =15pF	300	MHz
fmax	Input Frequency	CL = 5pF	600	MHz
fmax	Input Frequency	CL = 2pF	800	MHz

Notes:
1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

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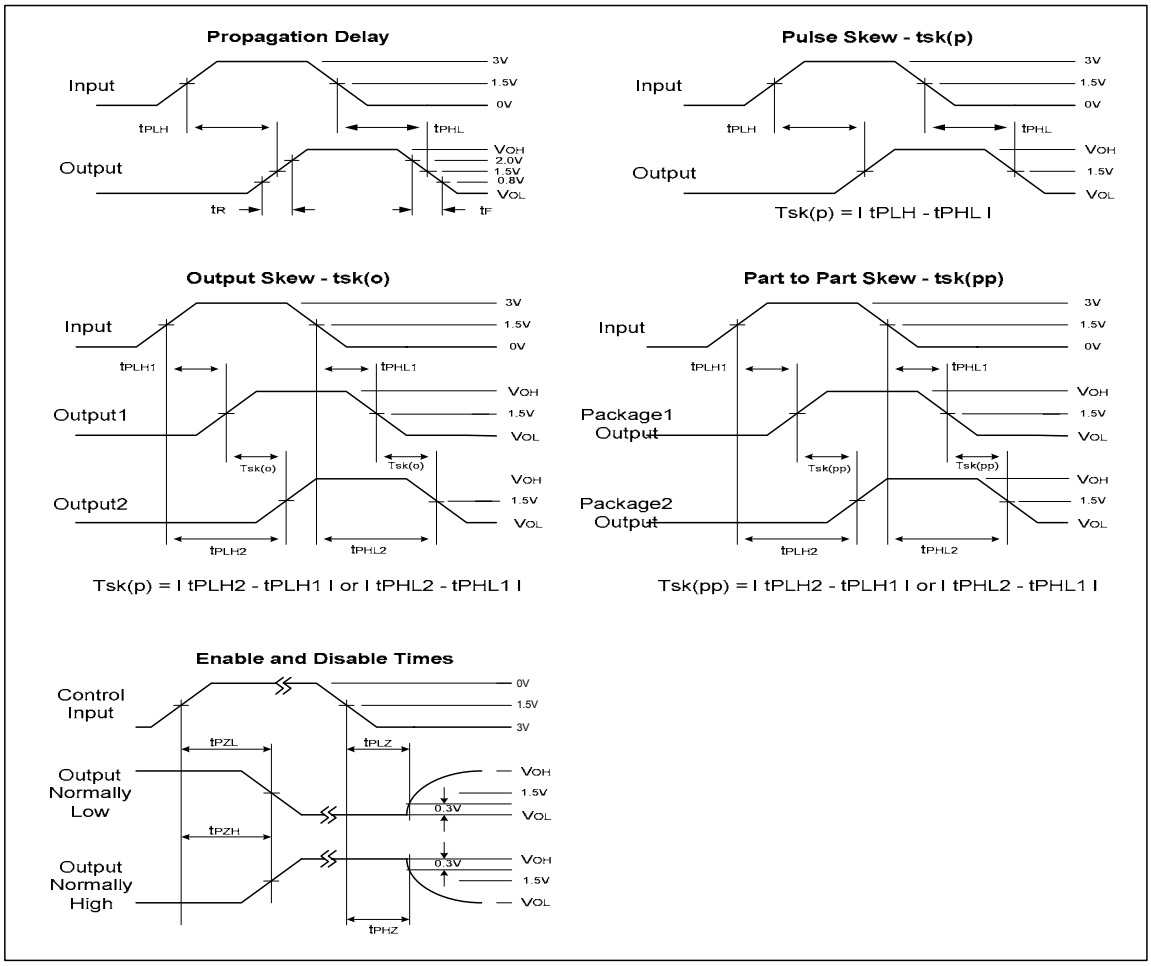
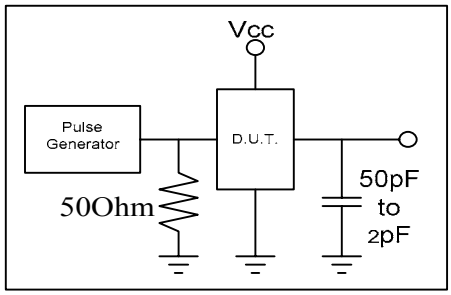
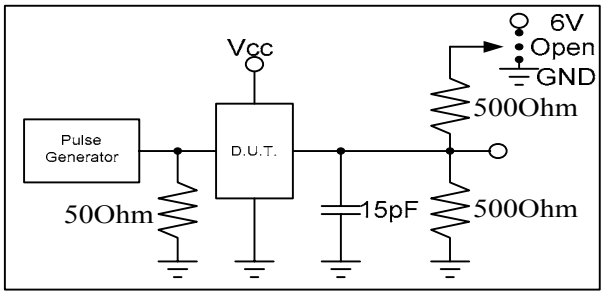
Test Waveforms



Test Circuit





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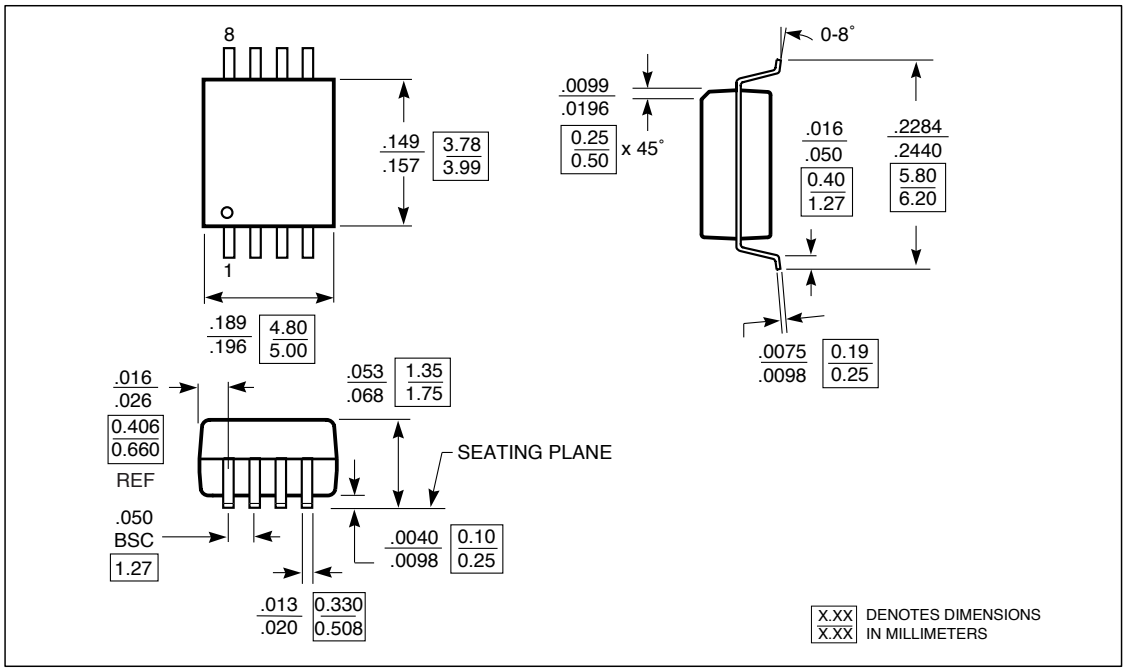
Packaging Mechanical Drawing: 8 pin SOIC



IC Ordering Information

Ordering Code	Package		Top-Marking	T_A
PO74G553ASU for Tube	8-pin 150mil SOIC	Pb-free & Green	PO74G553AS	-40°C to 85°C
PO74G553ASR for Tape & Reel	8-pin 150mil SOIC	Pb-free & Green	PO74G553AS	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER REEL	TAPE LEADER LENGTH	QTY PER TUBE
T	SOIC 8	12	8	Top Left Corner	39 (12”)	3000	64 (20”)	97