PO74HSTL85350A

LVCMOS Input to HSTL Output 1:4 Fanout Buffer

300MHz TTL/CMOS Potato Chip

FEATURES:

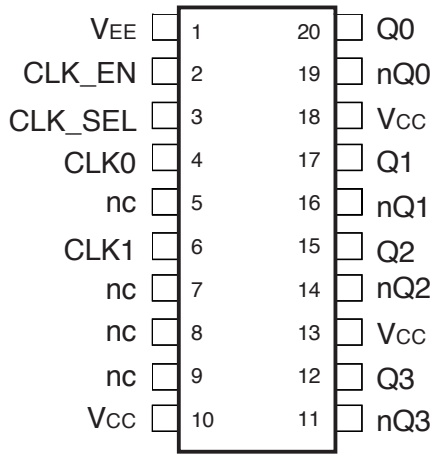
. Patented Technology
. Four HSTL differential outputs
. Two single LVTTL/LVCMOS inputs
. Operating frequency up to 300MHz with 15 pf load
. Very low output pin to pin skew < 50ps
. 3.4-ns propagation delay (max)
. 2.4V to 3.6V power supply
. Industrial temperature range: –40°C to 85°C
. 20-pin TSSOP package

DESCRIPTION:

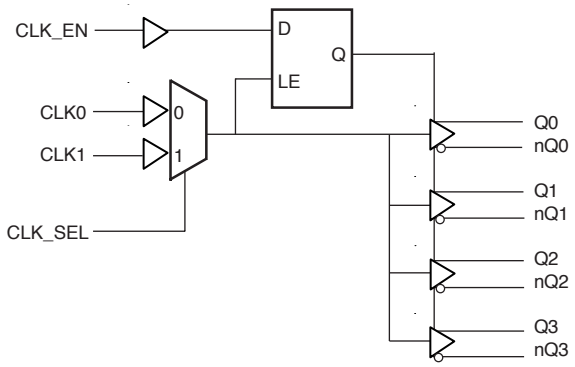
The PO74HSTL85350A is a low-skew, 1-to-4 differential fanout buffer targeted to meet the requirements of high-performance clock and data distribution applications. The device is implemented on CMOS technology and has a fully differential internal architecture that is optimized to achieve low signal skews at operating frequencies of up to 300MHz .

The device features two single-ended input paths that are multiplexed internally. This mux is controlled by the CLK_SEL pin. The PO74HSTL85350A functions as a signal-level translator and fanout on LVCMOS / LVTTL single-ended signal to four HSTL differential loads. Since the PO74HSTL85350A introduces negligible jitter to the timing budget, it is the ideal choice for distributing high frequency, high precision clocks across back-planes and boards in communication systems.

Pin Configuration



Logic Block Diagram



300MHz TTL/CMOS Potato Chip

Pin Definitions

Pin	Name	I/O	Type	Description
10,13,18	VCC	VCC	Power	Power supply, positive connection
5, 7, 8, 9	NC			No connect
3	CLK_SEL	I,PD	LVCMOS	Input clock select with pull down resistor
4	CLK0	I,PD	LVCMOS/ LVTTL	LVCOMS / LVTTL clock input
6	CLK1	I,PD	LVCMOS/ LVTTL	LVCOMS / LVTTL clock input
2	CLK_EN	I,PU	LVCMOS/ LVTTL	Clock enabled
1	VEE	GND	Power	Power Ground
19, 16,14,11	Q[0:3]#	O	HSTL	Complement output
20, 17,15,12	Q[0:3]	O	HSTL	Ture output

Control Input Function Table

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	nQ0:nQ3
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

Input/ Output Function Table

Inputs	Outputs	
CLK0 or CLK1	Q0:Q3	nQ0:nQ3
0	LOW	HIGH
1	HIGH	LOW

Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			88		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			88		KΩ

300MHz TTL/CMOS Potato Chip

Maximum Ratings

Description	Max	Unit
Storage Temperature	-65 to 150	°C
Operation Temperature	-40 to 85	°C
Operation Voltage	-0.5 to +4.6	V
Input Voltage	-0.5 to +5.5	V
Output Voltage	-0.5 to Vcc+0.5	V

Note:
stresses greater than listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability specification is not implied.

DC Electrical Characteristics

Symbol	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High voltage	Vcc=3V Vin=V_{IH} or V_{IL}, I_{OH}= -12mA	2.4	3	-	V
V_{OL}	Output Low voltage	Vcc=3V Vin=V_{IH} or V_{IL}, I_{OH}=12mA	-	0.3	0.5	V
V_{IK}	Clamp diode voltage	Vcc = Min. And I_{IN} = -18mA	-	-0.7	-1.2	V

Multiple Supplies: The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25 °C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. VoH = Vcc – 0.6V at rated current

300MHz TTL/CMOS Potato Chip

Power Supply Characteristics

Symbol	Description	Test Conditions (1)	Min	Typ	Max	Unit
Icc_Q	Quiescent Power Supply Current	Vcc=Max, Vin=Vcc or GND	-	0.1	30	uA

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, 25°C ambient.
3. This parameter is guaranteed but not tested.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

Switching Characteristics

Symbol	Description	Test Conditions (1)	Max	Unit
t_{PD}	Propagation Delay CLKA or CLKB to Output pair	CL = 15pF	3.4	ns
tr/tf	Rise/Fall Time	0.8V – 2.0V	0.8	ns
tsk(o)	Output Pin to Pin Skew (Same Package)	CL = 15pF, 125MHz	50	ps
tsk(pp)	Output Skew (Different Package)	CL = 15pF, 125MHz	350	ps
fmax	Input Frequency	CL =15pF	300	MHz

1. See test circuits and waveforms.
2. tpLH, tpHL, tsk(p), and tsk(o) are production tested. All other parameters guaranteed but not production tested.
3. Airflow of 1m/s is recommended for frequencies above 133MHz

Test Waveforms

FIGURE 1.
LVTTL/LVCMOS INPUT WAVEFORM DEFINITION

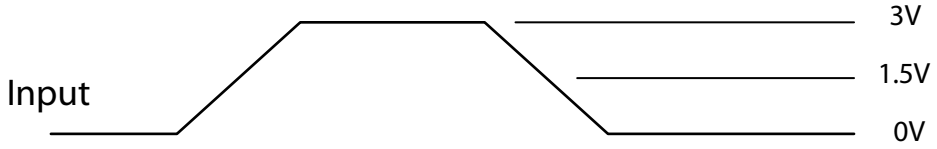


FIGURE 2.
HSTL OUTPUT

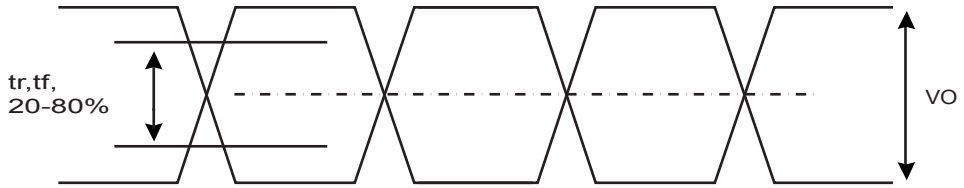


FIGURE 3.
Propogation Delay, Output pulse skew, and output-to-output skew for D to output pair

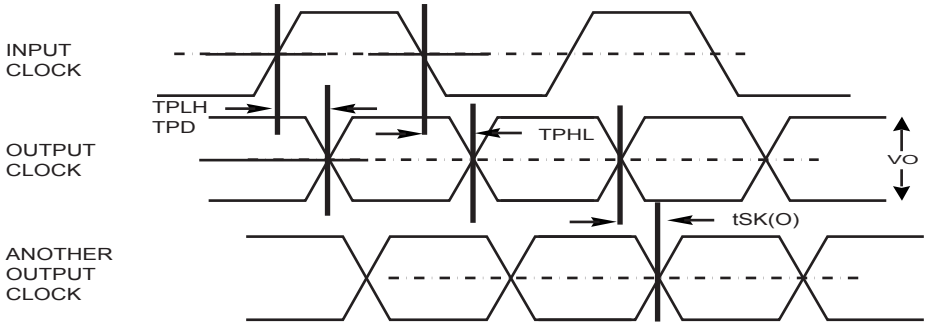
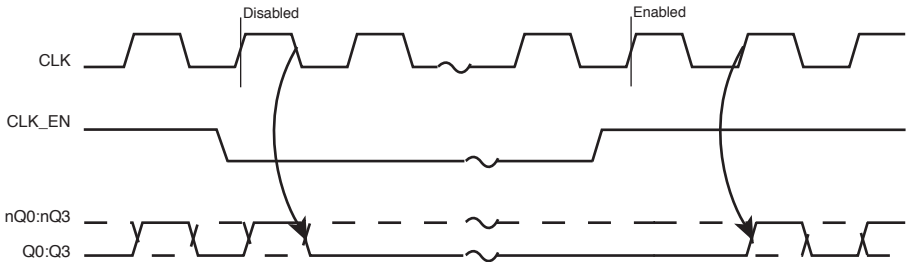
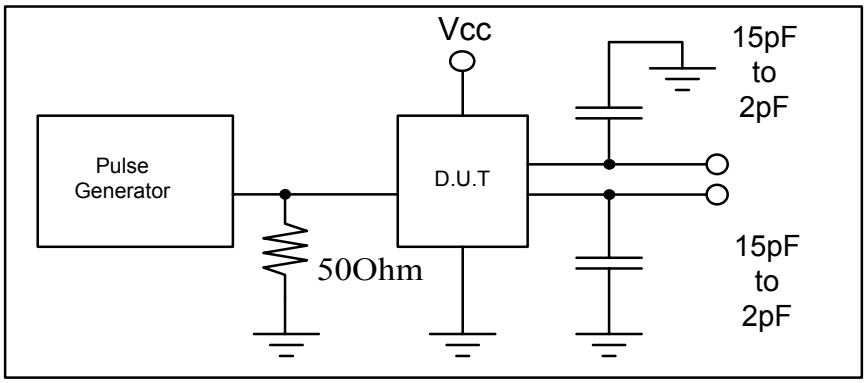


FIGURE 4.
CLK_EN Timing Diagram

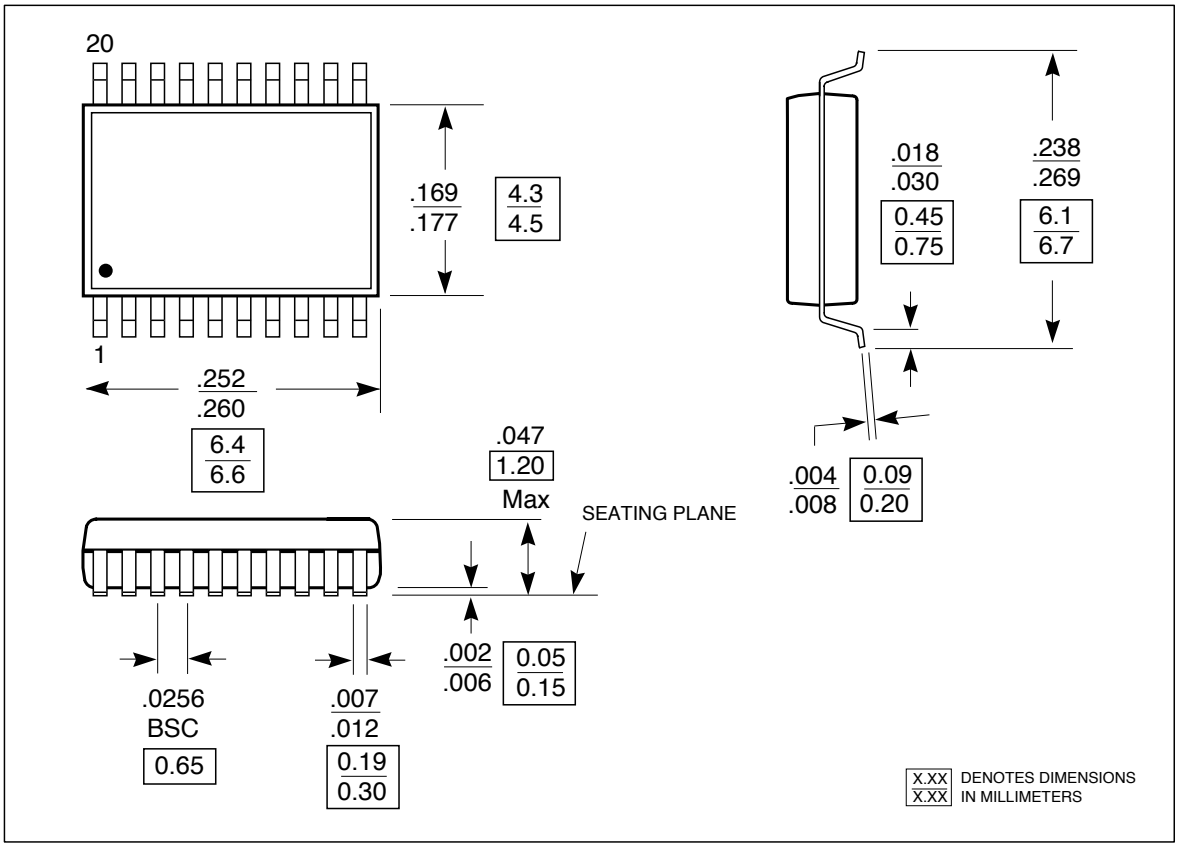


300MHz TTL/CMOS Potato Chip

Test Circuit



Packaging Mechanical Drawing: 20 pin TSSOP



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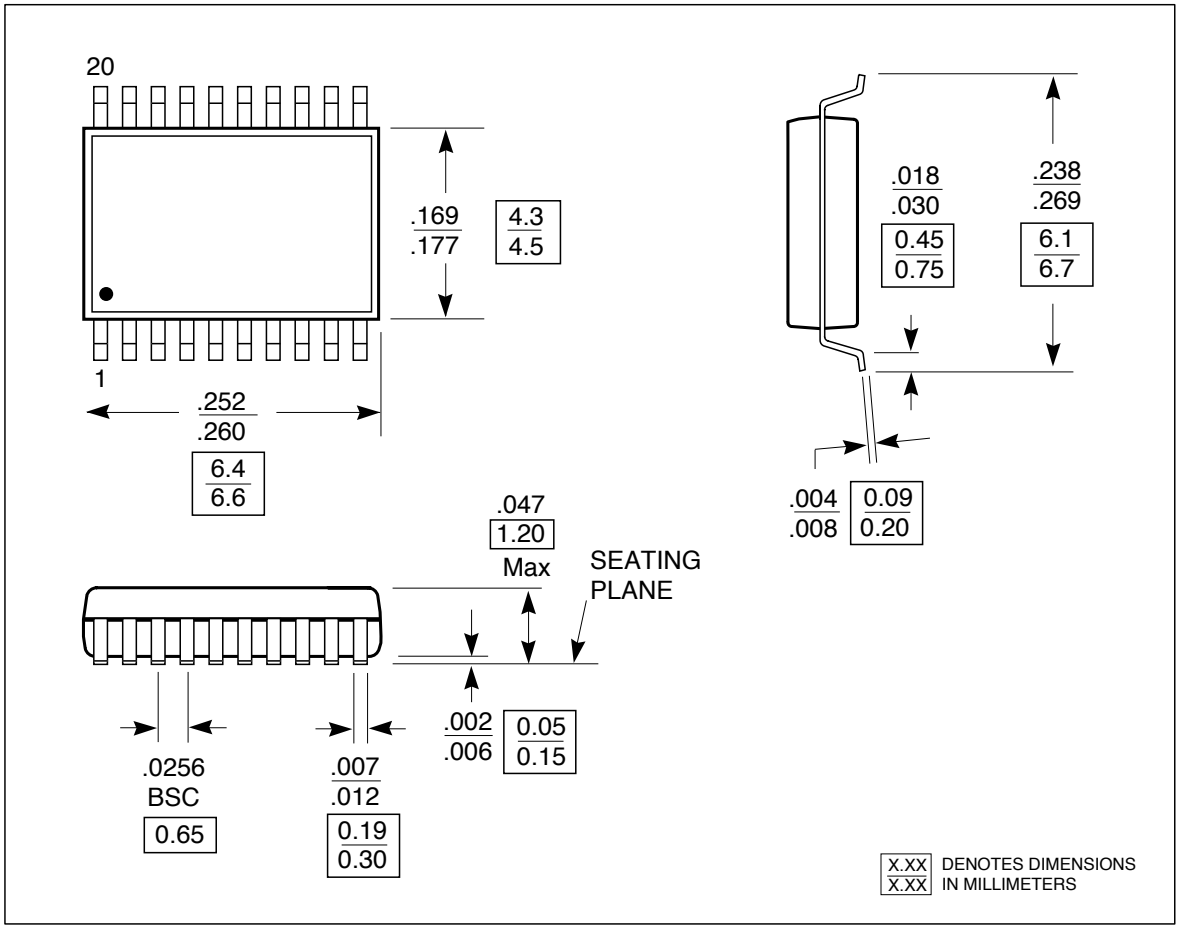

IC Ordering Information

Ordering Code	Package		Top-Marking	T_A
PO74HSTL85350ASU for Tube	20pin 173mil TSSOP	Pb-free & Green	PO74HSTL85350AS	-40°C to 85°C
PO74HSTL85350ASR for Tape & Reel	20pin 173mil TSSOP	Pb-free & Green	PO74HSTL85350AS	-40°C to 85°C

IC Package Information

PACKAGE CODE	PACKAGE TYPE	TAPE WIDTH (mm)	TAPE PITCH (mm)	TAPE & REEL PIN 1 LOCATION	TAPE TRAILER LENGTH	QTY PER TAPE	TAPE LEADER LENGTH	QTY PER TUBE
T	20pin 173mil TSSOP	16	8	Top Left Corner	39 (12″)	3000	64 (20″)	74