

## Application Note for Surface Mount Hermetic Package FDB Type

### 1. FDB type package general presentation

FDB type package is ideal for application requiring enhanced reliability and electrical performances. This surface mount square no lead package (QFN like) is fully hermetic and is designed to operate at very high frequency up to 30GHz with a very low thermal resistance at the same time.

This package is perfectly adapted to defense and space applications and can also be used for power devices.

Its very compact ceramic metal body with outline dimensions of 7x7 mm<sup>2</sup> is designed to be compatible with standard automatic SMT assembly and industrial tests equipments massively used for QFN packages.

This package includes two 50Ω accesses for millimeter-wave signals and twelve accesses for DC, control or RF signals. A large ground pad is managed at the package's bottom side in order to improve the electrical and thermal performances.

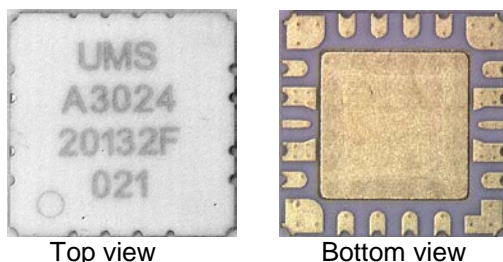


Figure 1: FDB package top and bottom views.

#### Main features:

	Unit	Typical Value
Package type	-	QFN metal-ceramic
Body dimensions	mm <sup>2</sup>	7 x 7
Package thickness	mm	1.5
Number of millimeter-wave leads	-	2
Number of low frequency leads	-	12
Metallic ground pad surface	mm <sup>2</sup>	4.7 x 4.7
Package's ground pad thermal resistance	°C/W	<0.2
MSL	-	1
Hermetic sealing (fine leak compliant Mil-Std-883 Method 1014.10 Condition A4, tracer gas He at 1atm)	ccHe/s/atm	1x10 <sup>-8</sup>
Package leads finish is gold (Au)	µm	0.8 min.
Solderability (Mil-Std-883 Method 2003.7, aging operation omitted)		Under x10 magnification, at least 95% coverage by continuous solder coating

## 2. Package outline

The package outline is given at the Annex 1.

Please periodically refer to the UMS web site: <https://www.ums-rf.com> to get the latest drawings.

## 3. Assembly recommendations

FDB type package is defined to be compatible with most of the standard surface mount assembly techniques (SMT). This section gives some recommendations to implement the package assembly on PCB.

### 3.1. Package bottom-side flatness

In despite of its large ground/thermal pad at the center, the bottom side of this package is very flat in order to ease the assembly process on PCB. The flatness between the large ground and the signal leads is better than  $\pm 50\mu\text{m}$  (see Figure 2).

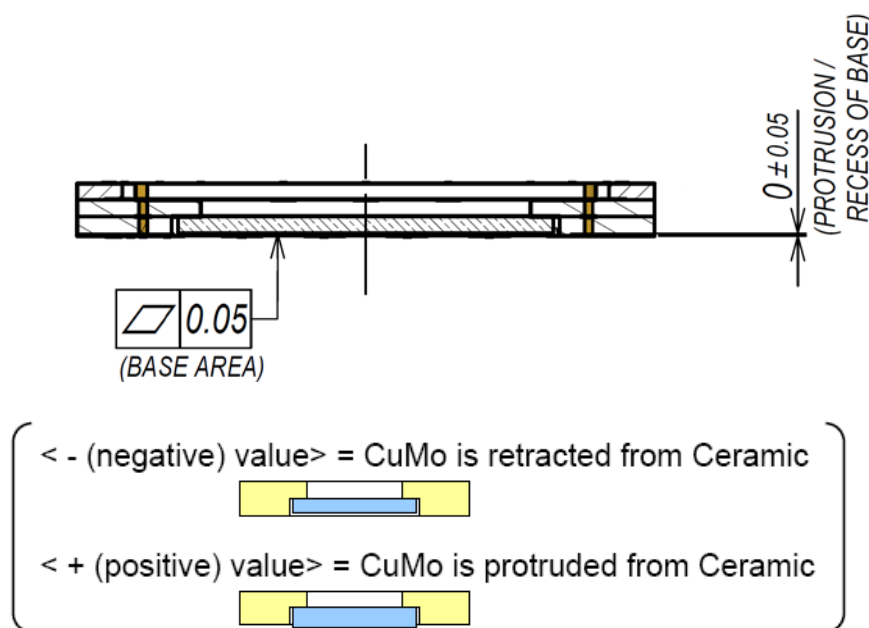


Figure 2: Package's bottom side flatness

### 3.2. Solder past selection

The FDB type package is designed to comply with standard surface mount assembly processes. Leadless (SnPb) or RoHS leadless solder pasts (like SnAgCu) can be used with this package which has gold plated terminations with 0.8 $\mu\text{m}$  minimum of gold (Au).

In case of a leadless solder past is selected (RoHS), an example of standard reflow profile is given at Figure 3. This profile is given for indication and has to be carefully adjusted depending on the actual PCB design and the selected solder past.

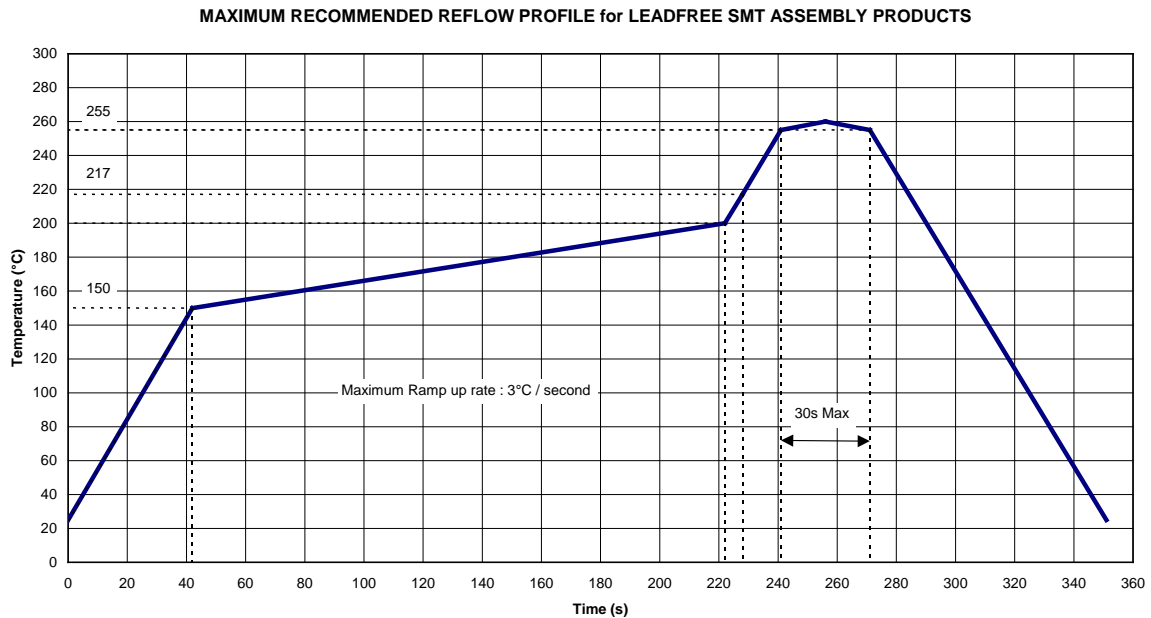


Figure 3 : Recommended reflow temperature profile for leadless solder (RoHS).

### 3.3. Recommendations for solder past printing process selection

Solder past deposition process and calibration should be defined according to the coplanarity parameters indicated at section 3.1. Three solder past deposition methods can be considered:

#### Dispensing

This process offers a lot of flexibility and is well adapted to medium production volume. The possibility to calibrate the amount of solder past dispensed on each land pattern enable to easily manage the coplanarity of the package's bottom side.

**Screen printing** and **stencil printing** processes are preferred for mass production. Apertures for screen and stencil design are critical and have to be done by considering the following parameters:

1. Land pattern dimensions on PCB. Generally a solder mask is also recommended to stop the solder during wetting.
2. Solder past viscosity
3. PCB design
4. Package leads and ground pad coplanarity

A design of experiment (DOE) is recommended in order to define the appropriated parameters.

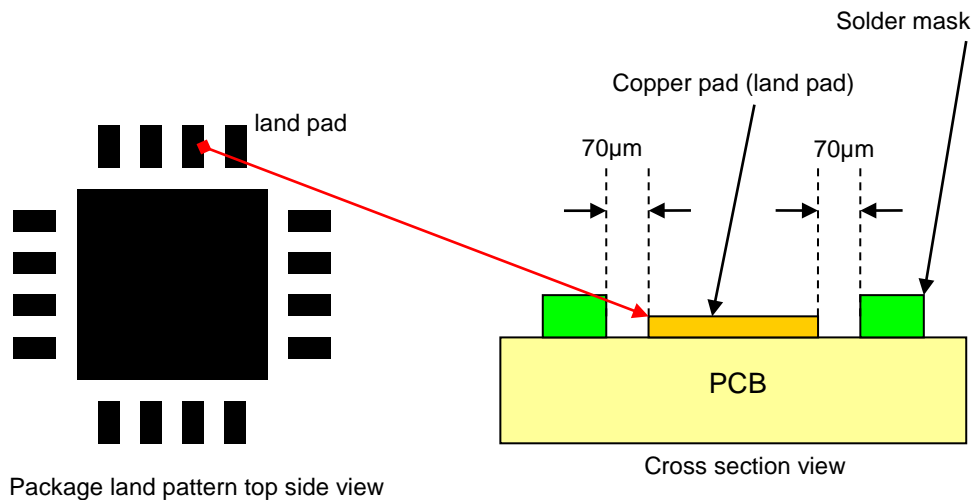
### 3.3.1. Solder mask design recommendations

For compact and low pitch packages it is necessary to prevent the solder bridging. Generally, a solder mask is used to avoid this kind of issues in production. The solder mask will also help to define the areas where the solder can flow and control the solder homogeneity under the package contacts (leads and exposed pad). Then the quality and the reliability of the solder joins are enhanced.

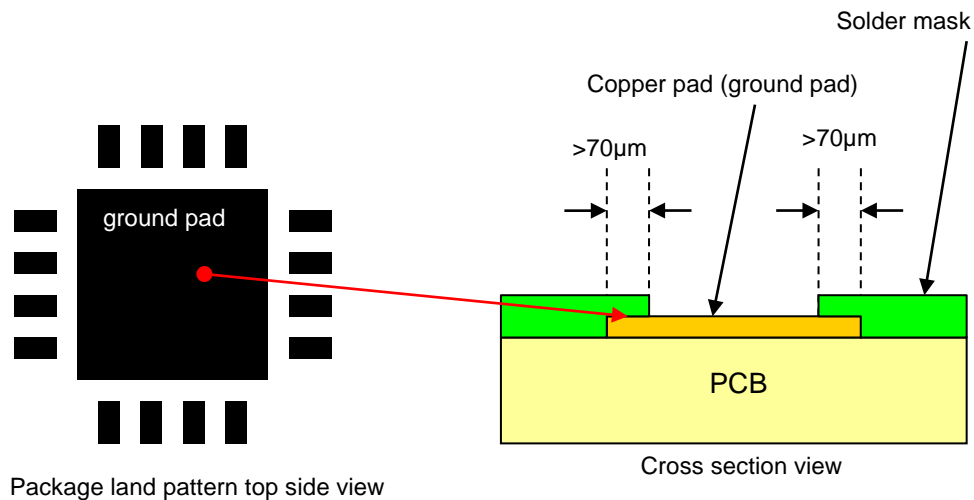
The recommended solder mask clearance around the copper pads on the PCB for land pads is 70µm [2.8mils] as shown on the Figure 4.

Concerning the package ground pad, it is recommended to manage an overlap of 70µm [2.8mils] minimum on the solder mask over the copper pad (see Figure 5). This configuration is suitable for self-centring of the package on the PCB foot-print during reflow process.

*Remark: The information given in this paragraph are only indicative and should not replace the design rules of the PCB manufacturer. Furthermore, the solder mask design must also take into account the final SMT assembly process used for module as well as the selected solder past characteristics.*



**Figure 4 : Solder mask clearance around the land pads.**



**Figure 5 : Solder mask clearance around the ground pad.**

### 3.3.2. Stencil printer recommendations

The choice of the stencil printer is very critical and must be done by the SMT assembler. The design of the stencil should be done in accordance with the solder paste material selected and the printing equipment capability. The guide lines given below are very general and only the assembler's design rules might be considered for the product industrialization.

The solder paste deposition for a small pitch package is very sensitive to the process, and should fit with the deposition on very small surfaces like the land pads (lead contact surface is less than 0.1mm<sup>2</sup>) but also on large surfaces as for the ground pad.

The squeegee blade used to deposit the solder paste into the stencil cavities could bend in the larger cavities and then limit the amount of solder paste deposited. A very convenient method used to solve this issue is to split the exposed pad surface into an array more compatible with the smallest zones defined for the land pads.

Generally the stencil aperture opening above the land pad is smaller than the copper land pad (about 50µm [2 mils] in the two directions, see Figure 6).

The stencil design for the ground pad region results from trials and evaluations on pre-serial batches in order to define the optimum pattern. Two examples of configuration are given on Figure 7.

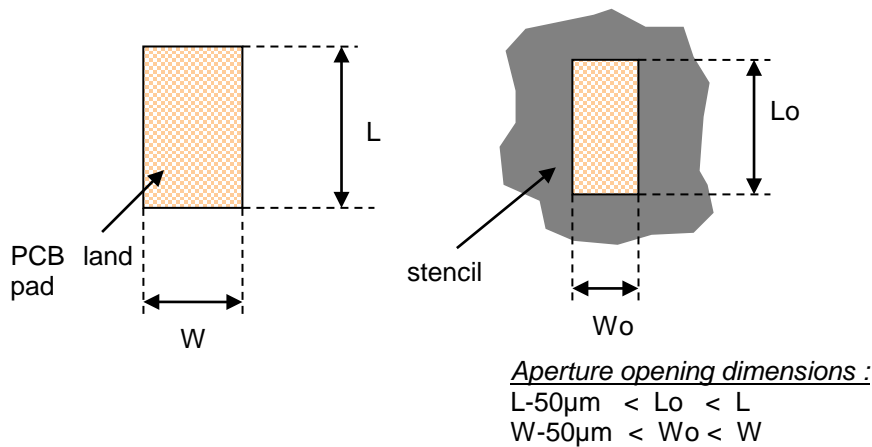


Figure 6 : Stencil aperture opening for land pads.

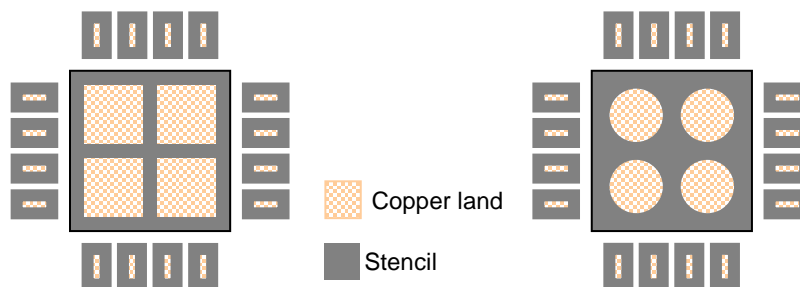


Figure 7 : ground pad stencil examples.

Take the following items into account when setting the solder paste supply amount:

1. **Solder paste printing thickness:**

In setting the solder paste printing thickness, consider the planarity of the package pins and investigate the minimum solder paste printing thickness as follows.

Minimum solder paste printing thickness = Package pin coplanarity + 0 to 30  $\mu\text{m}$

2. **Solder paste printing diameter:**

In setting the solder paste printing diameter, take the following items into consideration. Provide a stencil aperture spacing of at least 0.3 mm to prevent the occurrence of solder bridges. To prevent open solder connections, set the solder paste printing diameter to be a value larger than the minimum solder paste printing thickness as stipulated above.

## 4. Recommended PCB design

A demonstration printed circuit board design is available (PCB reference is 503475) and has been designed to achieve excellent electrical performances up to 30GHz. For cost improvement this PCB is made of Rogers Ro4003 material 0.203 mm [8 mils] with a double side copper cladding of 17 $\mu$ m [0.7 mils]. In this design, the package ground pad is electrically and thermally grounding with 49 via-holes made through the Ro4003 dielectric layer (see Figure 8). Quasi-coplanar ground/signal/ground 50 $\Omega$  accesses are managed on the PCB at contact area of the package's millimeter-wave leads in order to improve the impedance matching at high frequency. Decoupling SMD capacitors have to be located as close as possible from the packaged device in order to prevent any un-stability or spurious issue. The exact location depends on the product, the application and of the selected PCB design. The detailed PCB drawing is given at the Annex 2. A dxf file version can be provided upon request.

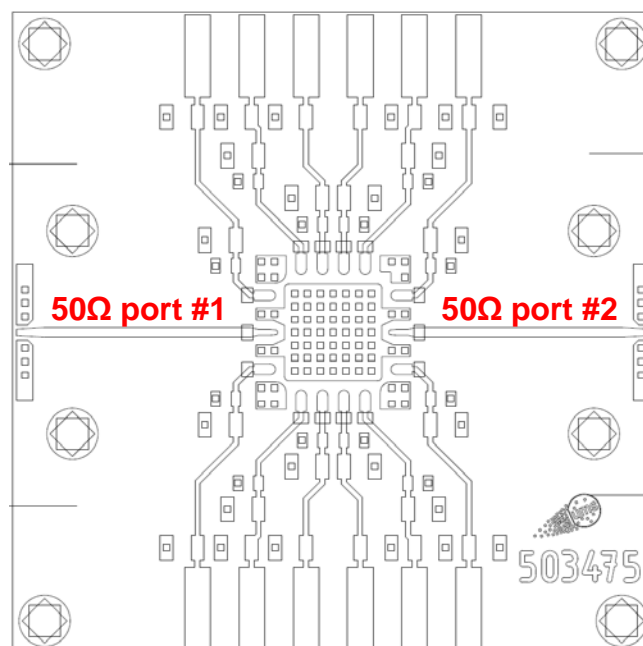
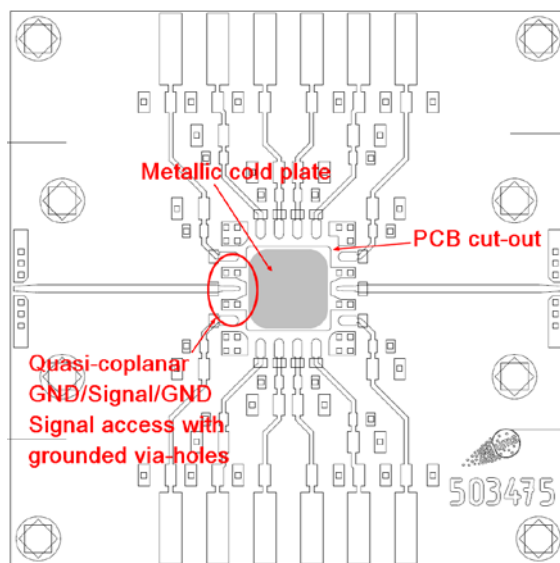


Figure 8 : Recommended PCB electrical design.

For enhanced thermal performances, a cut-out in the PCB can also be recommended in order to braze directly the package's ground pad on the metallic cold plate (ie. heat sink) of the system (see the example at Figure 9).



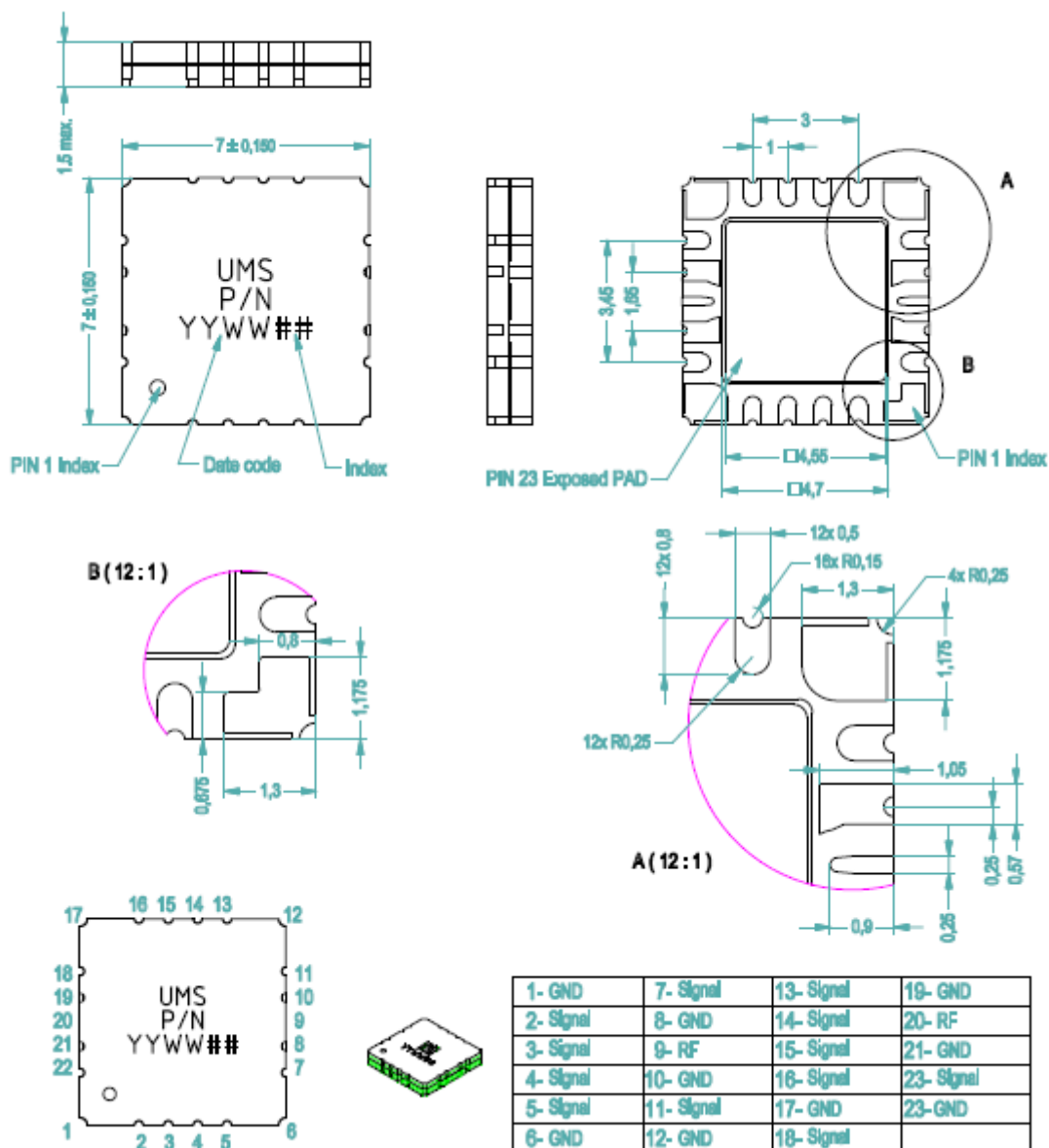
**Figure 9: Alternative PCB configuration with metallic heat sink rising in the PCB cut-out.**

Thanks to its construction, the FDB package is perfectly mechanically matched with LTCC or others ceramic boards which should have very similar thermal expansion coefficient (CTE in ppm/°C). These boards families are perfectly adapted to space or military applications.

For organic PCBs made of FR4 or other multi-layers thick laminated substrates, and especially for hardened applications with large temperature range, thermal expansion of the mother-board has to be considered during the system design. In some cases, package under-filling could be recommended to improve the mechanical reliability of the assembly. Underfilling materials NAMICS Ohmcoat 1570, 1572 could be proposed.

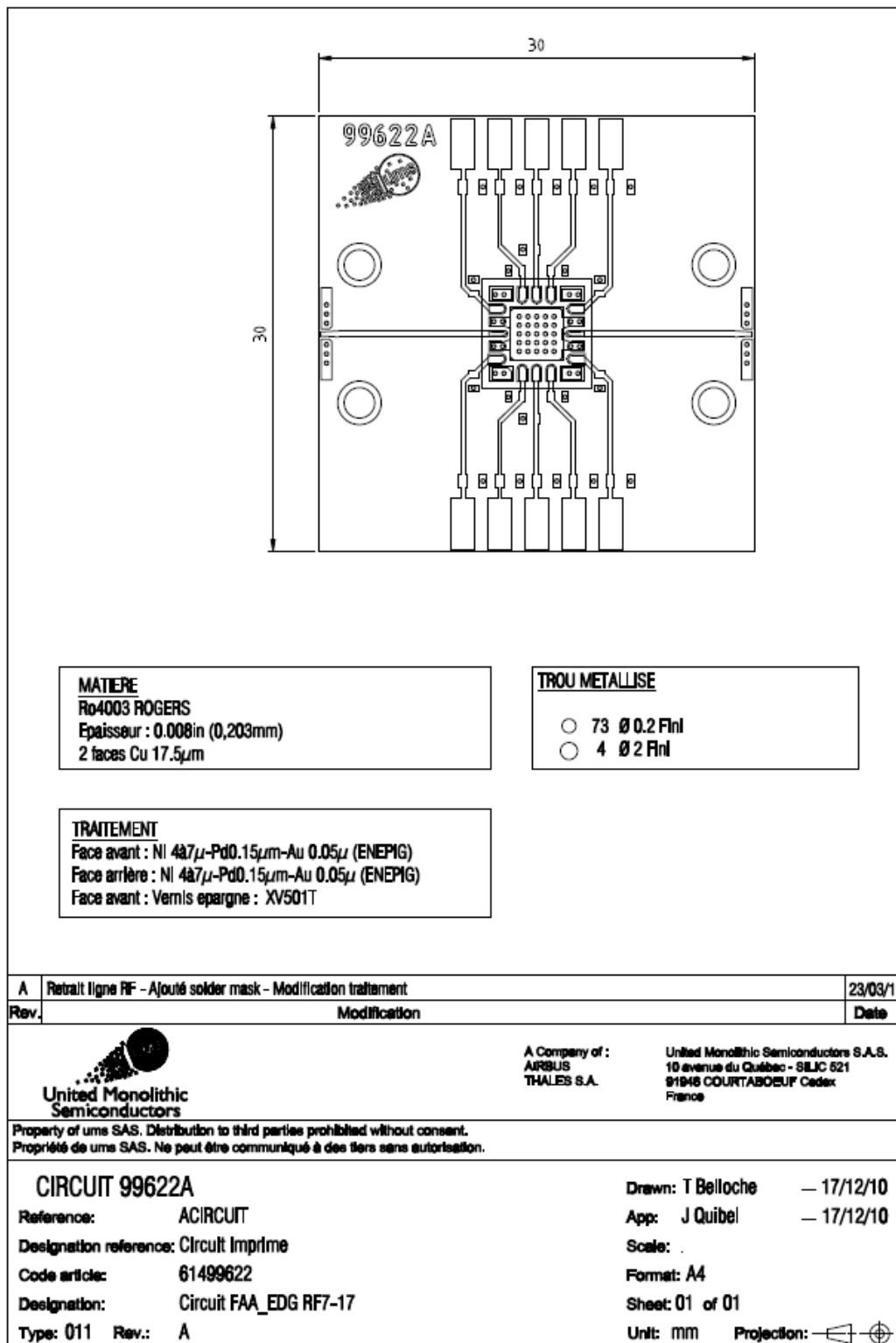


## 5. ANNEX 1: FDB package outline



Unit : mm

## 6. ANNEX 2: Recommended PCB electrical design



## 7. Glossary

SMD:	Surface Mount Device
SMT:	Surface Mount Techniques
QFN:	Quad Flat Non-leaded
PCB:	Printed Circuit Board
BOM:	Bill Of Materials
Sij:	Scattering Parameters
RoHS:	Restriction of the use of certain Hazardous Substances
Lead-free:	Part of the RoHS directive (Leadless)
DI:	Deionised water
MMIC:	Monolithic Microwave Integrated Circuit
THB:	Temperature and Humidity Biased
HOTL:	High Temperature Operating Life
Pb:	Lead
MSL:	Moisture Sensitivity Level
CTE:	Coefficient of thermal expansion
CPK:	Or CpK is a process capability index.

## 8. References

[1]: Mil-Std-883

## Recommended package footprint

Refer to the application note AN0017 available at <https://www.ums-rf.com/> for package foot print recommendations.

## SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

## Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACH N°1907/2006. More environmental data are available in the application note AN0019 also available at <https://www.ums-rf.com/>.

## Recommended ESD management

Refer to the application note AN0020 available at <https://www.ums-rf.com/> for ESD sensitivity and handling recommendations for the UMS package products.

## Contacts:

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